Industrial Electronics

Prepared By:
Ajit Singh, Lecturer

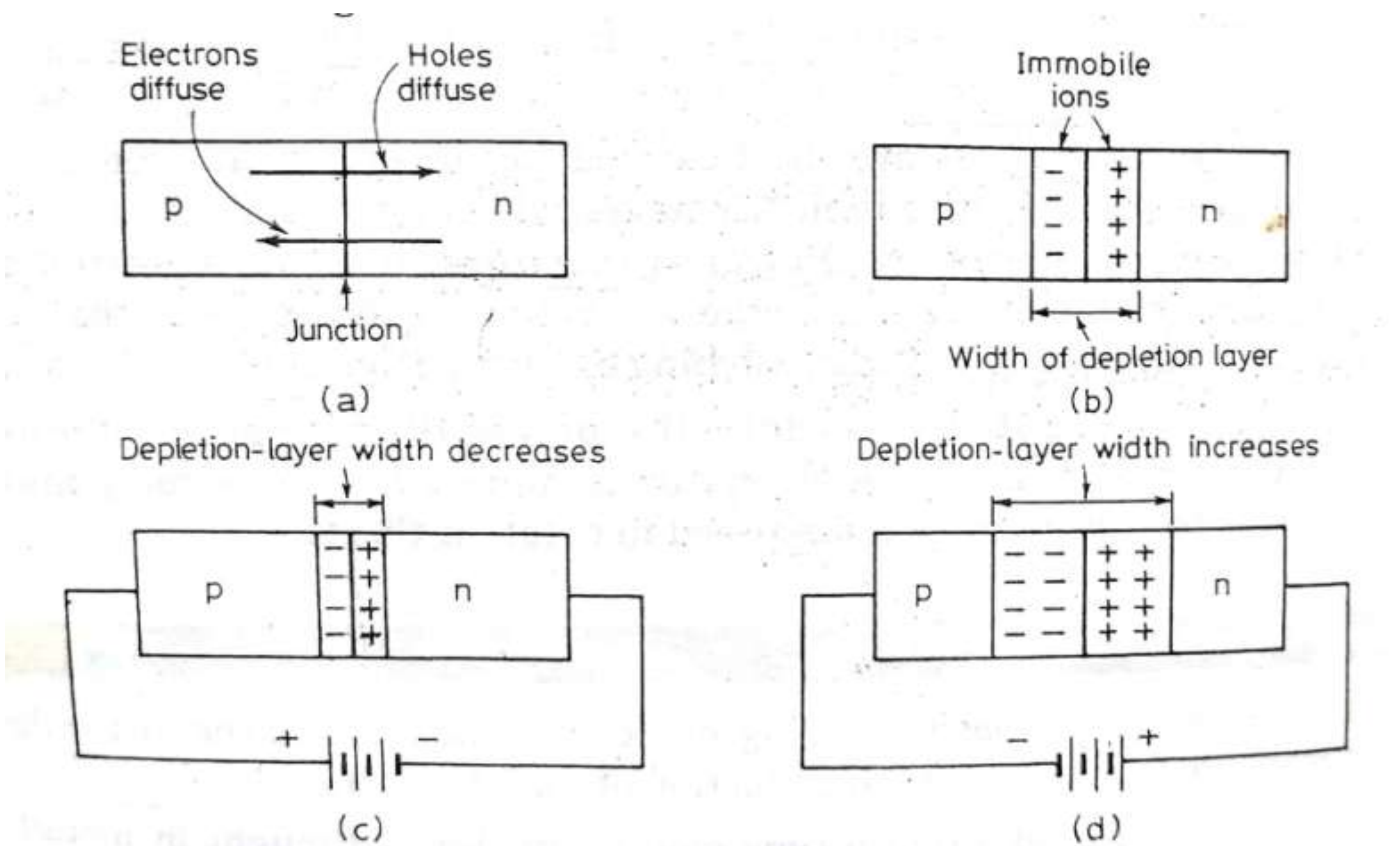
The p–n Junction

- A p–n junction is formed when p–type semiconductor is brought in metallurgical or physical contact with n–type semiconductor.
- p–region has more holes concentration.
- n– region has more electrons concentration.

The p-n Junction

- In p-region holes are majority carriers and electrons are minority carriers.
- In n-region electrons are majority carriers and holes are minority carriers.

Depletion Layer



Types of Diode

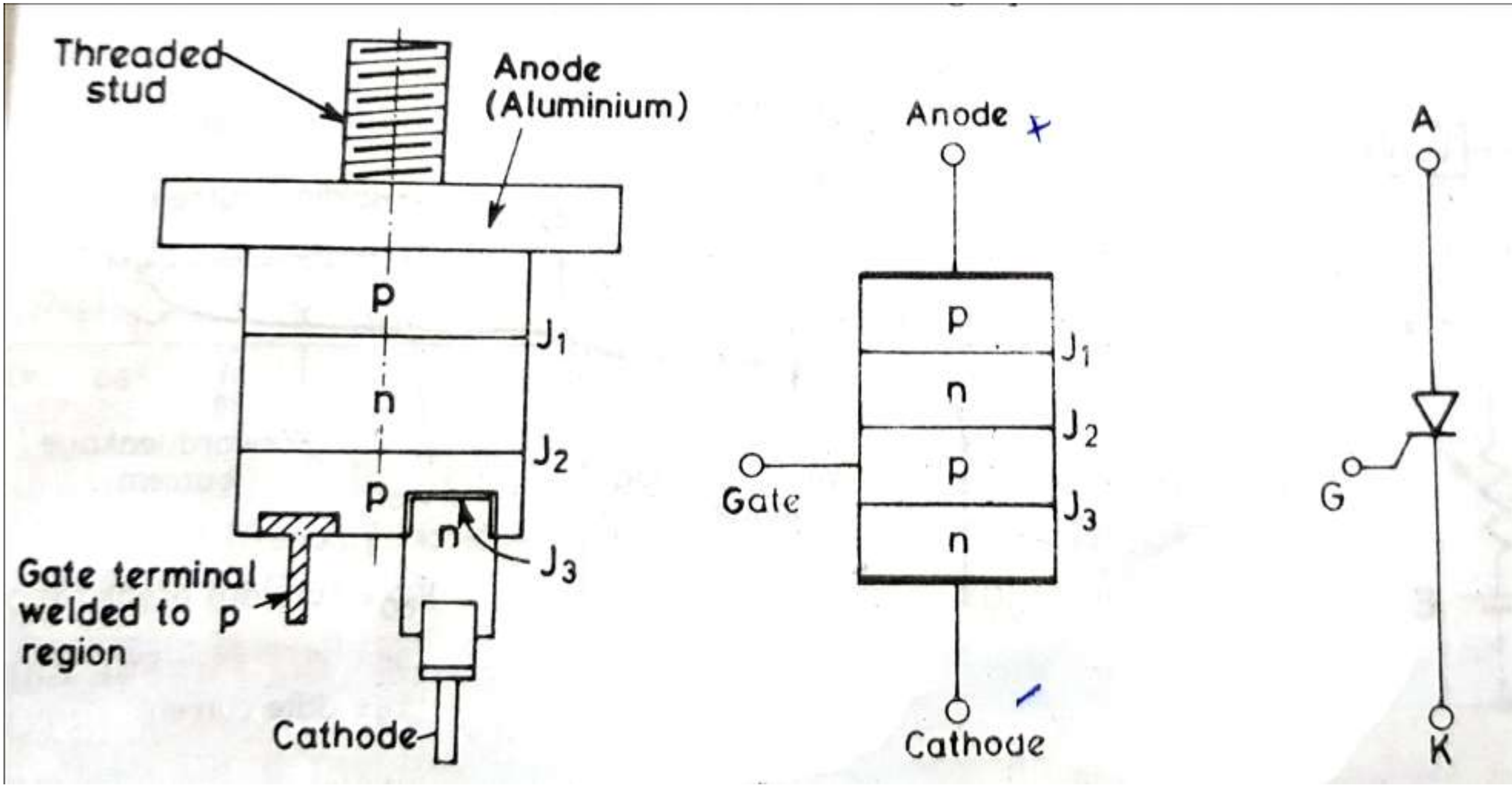
Thyristor

- The term Thyristor denotes a family of semiconductor devices used for power control in DC and AC system.
- Thyristor is a family of semiconductor devices like SCR, TRIAC, Diac, Slicon controlled Switch (SCS), Programmable Unijunction Transistor (PUT) etc.
- The use of SCR is so vast that over the years, the word thysristor has become synonymous with SCR.

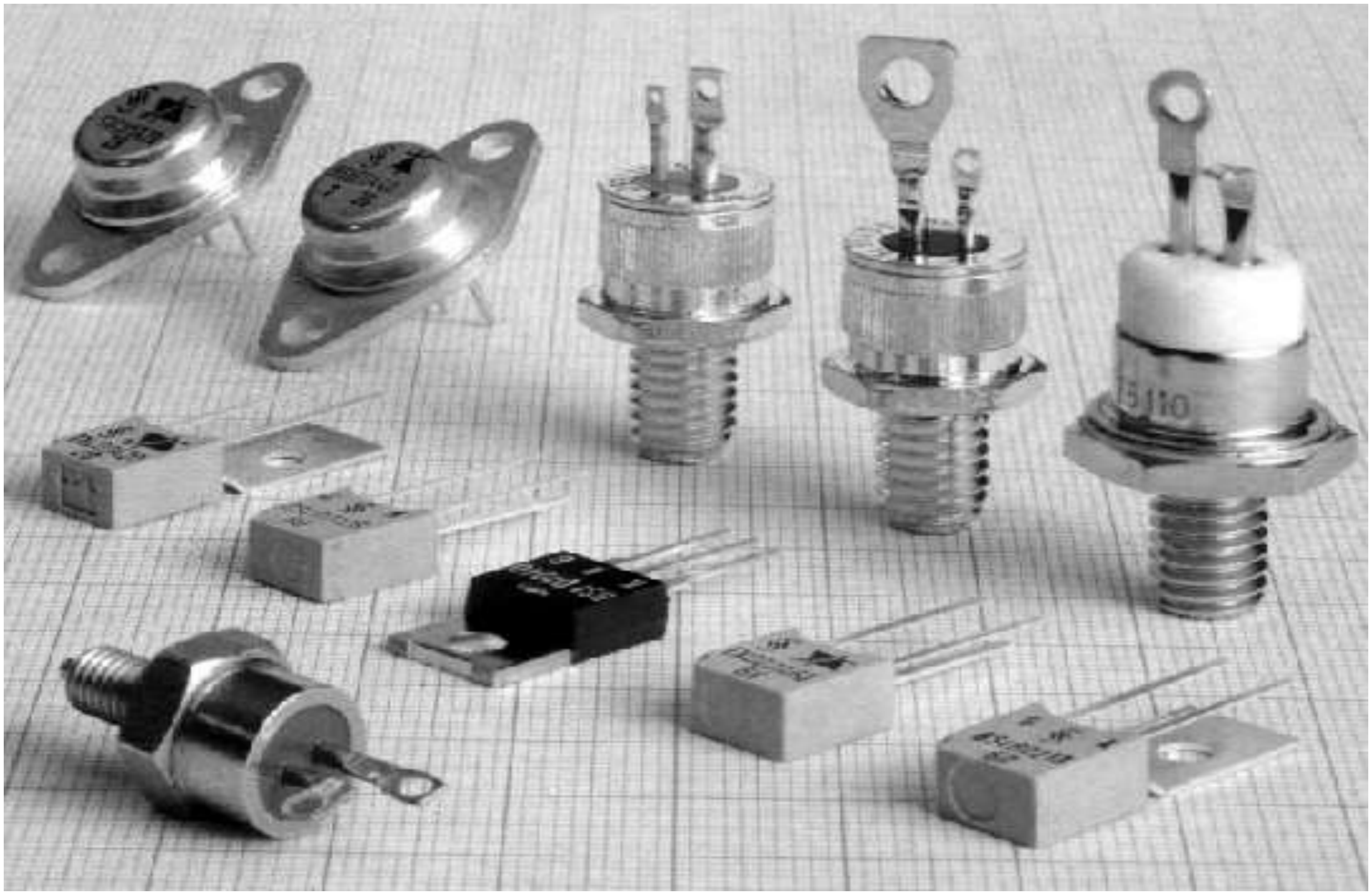
Thyristor

- Thyristor has characteristics similar to a thyratron tube.
- The name Thyristor is derived from combination of THYRatron and transISTOR.
- Thyristor:
  - Constitutes three or more p-n junctions.
  - Has two stable states, an ON state and an OFF state.
  - Can change its state from one to another.

SCR (Silicon Controlled Rectifier)




8645
TIC106D



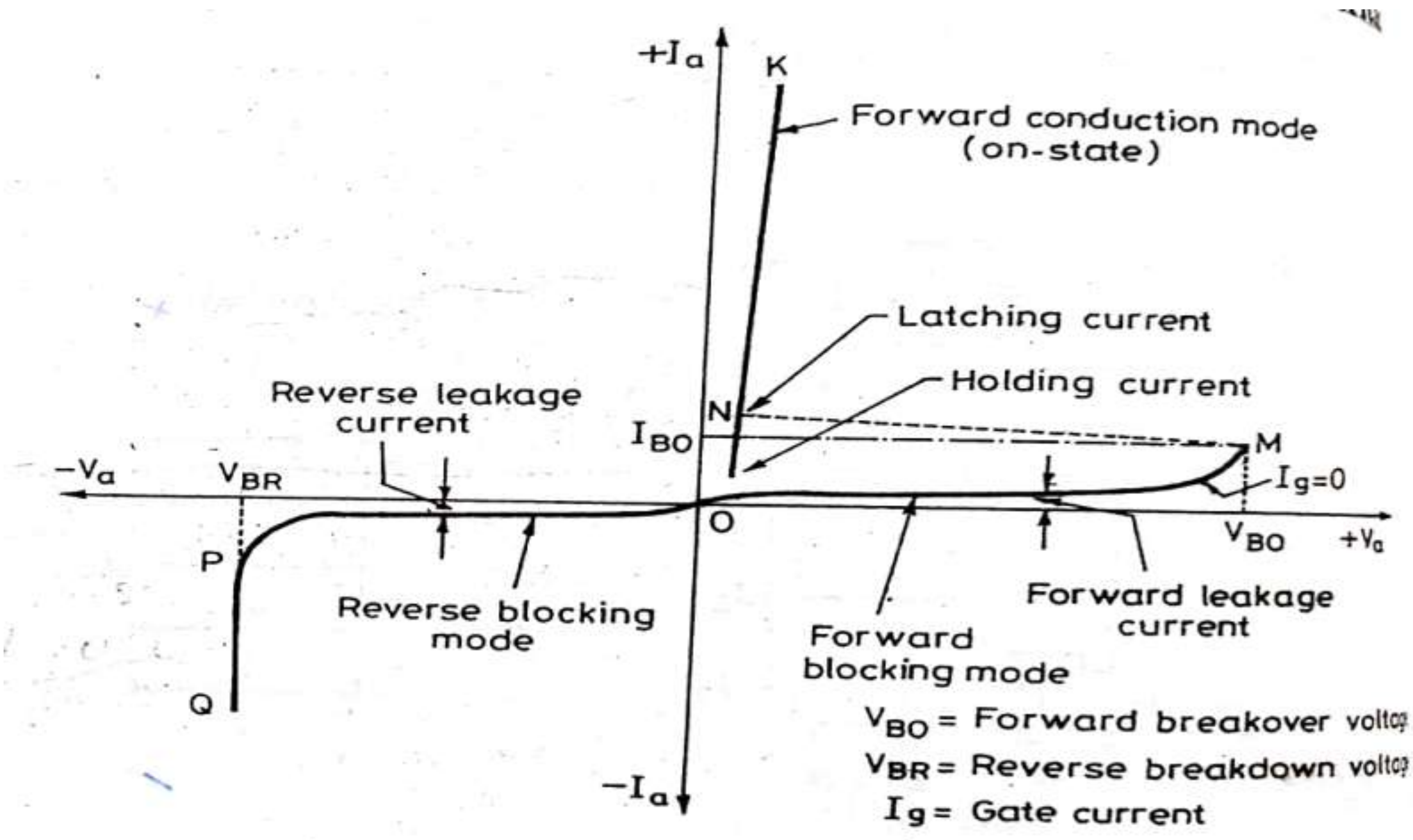
Thyrister (SCR)

- It is four layer, three junction, p-n-p-n semiconductor switching device.
- It has three terminals; Anode, Cathode and Gate.
- Gate terminal is usually kept near cathode terminal.
- SCRs of voltage rating 10 kV and rms current rating of 3000A with corresponding power handling capacity of 30MW are available.

Thyrister (SCR)

- SCR is so called because silicon is used for its construction and used as controlled rectifier.
- Unlike diode, a thyristor also blocks the current flow from anode to cathode until it is triggered by gate signal.

SCR Characteristics



SCR Characteristics

- Forward Blocking Mode
  - Anode is made +ve w.r.t. Cathode , Gate open.
  - $J_{1,}$ J_3 are forward biased, J_2 is reverse biased.
  - Forward leakage current flows.
  - SCR offers high impedance.
  - It can be treated as an open switch.

SCR Characteristics

- Forward Conduction Mode
  - When anode to cathode forward voltage is increased, Junction J_2 will have an avalanche breakdown at Forward Break over Voltage V_{BO}.
  - Voltage drop across the thyristor is of the order of 1 to 2 V, depending on SCR rating.
  - Anode current is limited by load impedance.
  - Thyristor acts as a closed switch.

SCR Characteristics

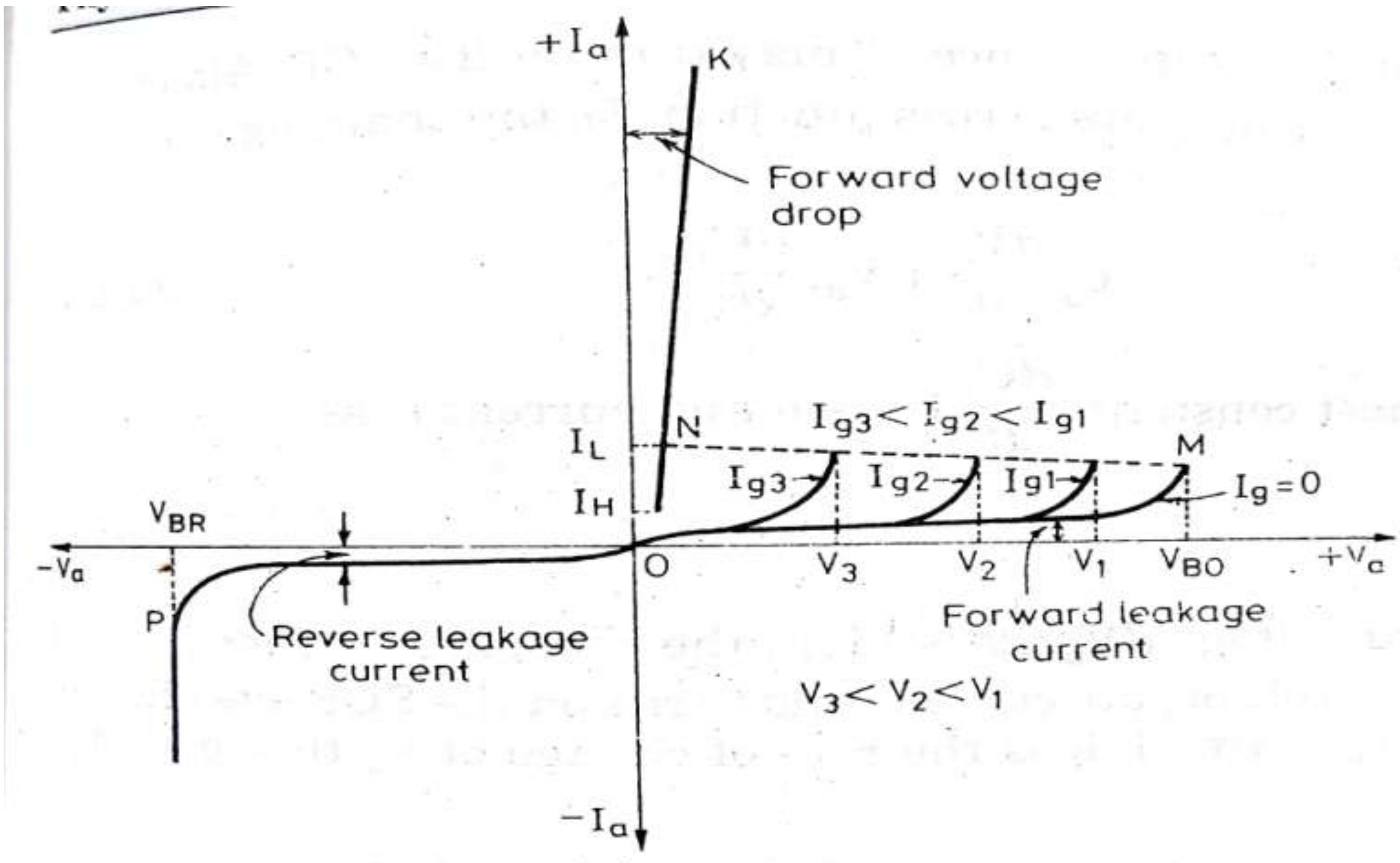
- Reverse Blocking Mode
  - Cathode is made +ve w.r.t. Anode, Gate open.
  - J_1, J_3 are reverse biased, J_2 is forward biased.
  - Device behaves as two diodes connected in series with reverse voltage applied.
  - Reverse leakage current of few milli amperes flow.
  - At reverse breakdown voltage V_{BR}, an avalanche occurs at J_1 and J_3.
  - Reverse current increases rapidly.
  - Large current with V_{BR} gives rise to more losses.
  - This may lead to damage of SCR.

SCR Characteristics

- Gate Triggering
  - Simple, reliable and efficient method to turn on the SCR and is mostly used.
  - Positive gate voltage between gate and cathode is applied.
  - Charges are injected in to inner p layer
  - The voltage at which forward break over occurs, is reduced.
  - Higher the gate current, lower is the forward break over voltage.
  - Typical gate current is 20 to 200 mA.

- Gate Triggering Continued…
  - With positive gate current, p layer is flooded with electrons from cathode as n layer is heavily doped as compared to gate p layer.
  - Some of these electrons reach junction J_2.
  - Due to this, width of depletion layer near junction J_2 is reduced and it breaks down at lower voltage.
  - Reverse biased junction J_2 no longer exists.
  - If gate current is removed, anode to cathode current remains unaffected.

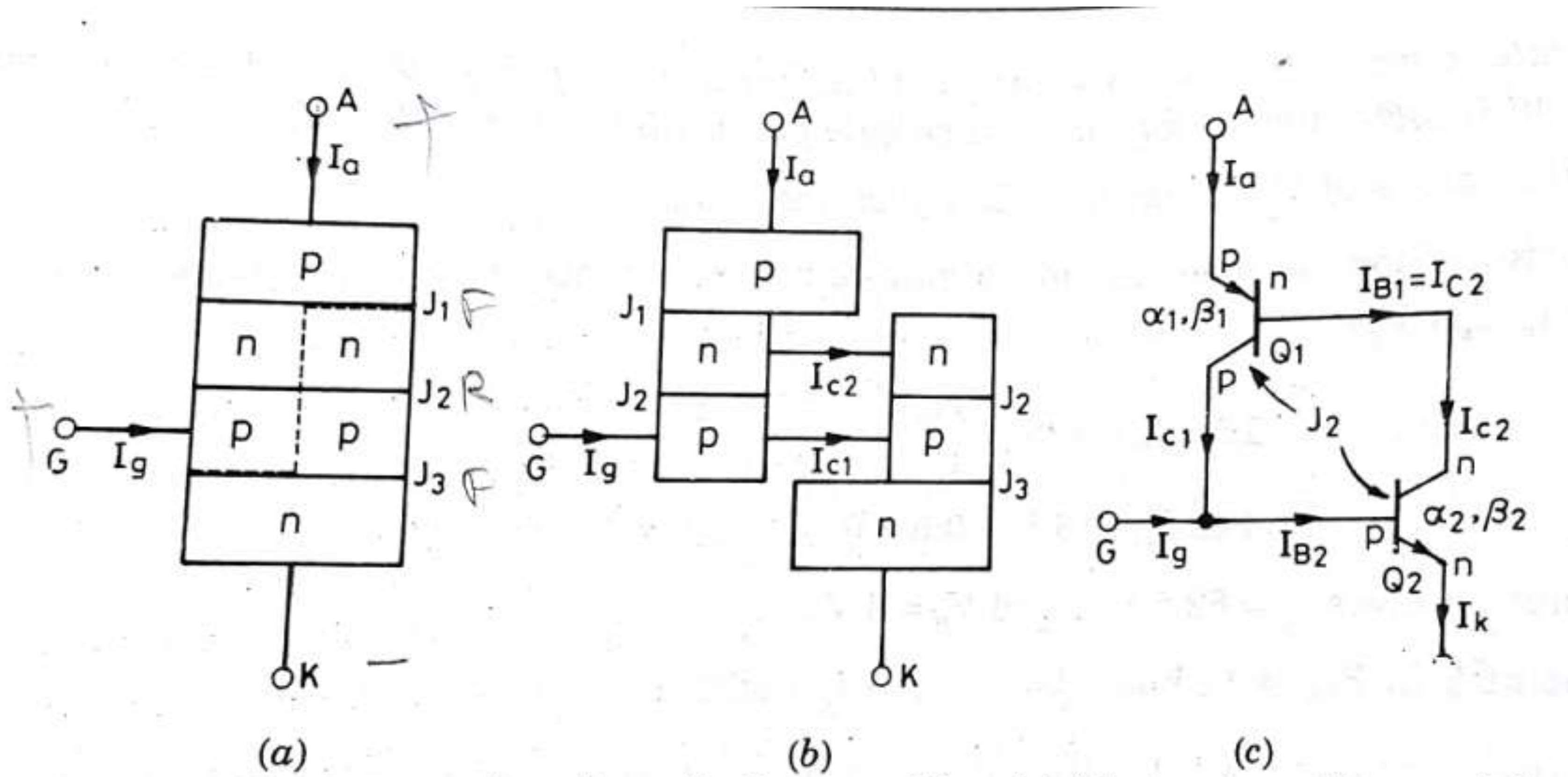
SCR Characteristics



- Latching Current:
  - Minimum value of anode current which SCR must attain during turn on process, to maintain conduction when gate signal is removed.
- Holding Current:
  - Minimum value of anode current below which it must fall for turning off the thyristor.

  - Latching current is associated with turn on process and Holding current with turn off process

Two Transistor Analogy



Two Transistor Analogy

circuit ...

In the off-state of a transistor, collector current I_C is related to emitter current I_E as

$$I_C = \alpha I_E + I_{CBO}$$

where α is the *common-base current gain* and I_{CBO} is the common-base leakage current of collector-base junction of a transistor.

For transistor Q_1 in Fig. , emitter current I_E = anode current I_a and I_C = collector current I_{C1}. Therefore, for Q_1,

...(i)

$$I_{C1} = \alpha_1 I_a + I_{CBO1}$$

where α_1 = common–base current gain of Q_1

and I_{CBO1} = common–base leakage current of Q_1.

Two Transistor Analogy

Similarly, for transistor Q_2, the collector current I_{C2} is given by

$$I_{C2} = \alpha_2 I_k + I_{CBO2} \quad \text{....(ii)}$$

where α_2 = common–base current gain of Q_2

I_{CBO2} = common–base leakage current of Q_2

and I_k = emitter current of Q_2.

The sum of two collector currents given by Eqs. (i) and (ii) is equal to the external circuit current I_a entering at anode terminal A.

$$\therefore \quad I_a = I_{C1} + I_{C2}$$

or

$$I_a = \alpha_1 I_a + I_{CBO1} + \alpha_2 I_k + I_{CBO2} \quad \text{.(iii)}$$

When gate current is applied, then $I_k = I_a + I_g$. Substituting this value of I_k in Eq. (iii) gives

$$I_a = \alpha_1 I_a + I_{CBO1} + \alpha_2 (I_a + I_g) + I_{CBO2}$$

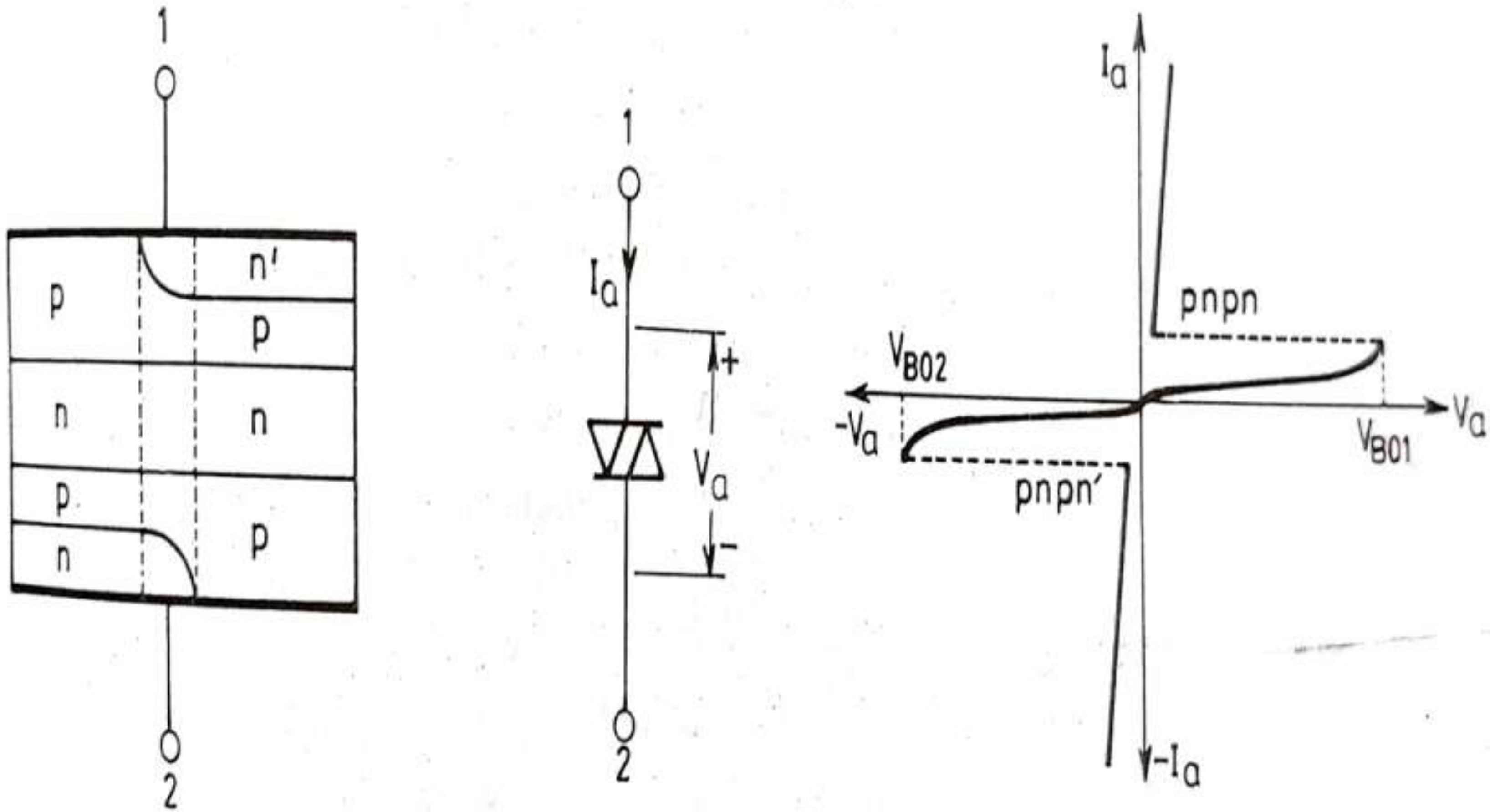
or

$$I_a = \frac{\alpha_2 I_g + I_{CBO1} + I_{CBO2}}{1 - (\alpha_1 + \alpha_2)}$$

Two Transistor Analogy

- For a silicon transistor, current gain α is very low at low emitter current.
- With an increase in emitter current, α builds up rapidly.
- With $I_g=0$, $(\alpha_1 + \alpha_2)$ is very low.
- If emitter current is increased so that $(\alpha_1 + \alpha_2)$ approaches unity, I_a would tend to become infinity.

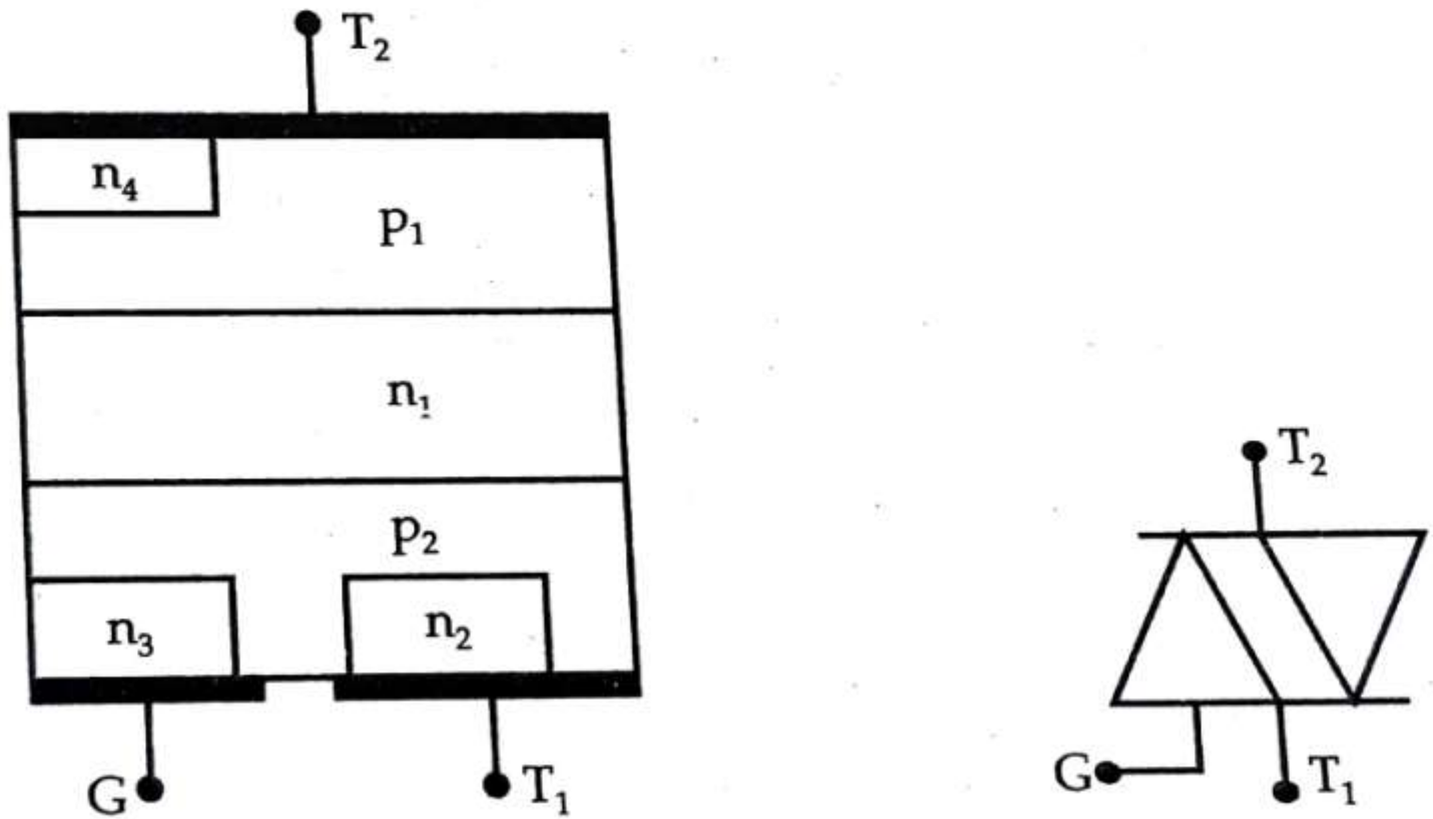
DIAC



DIAC

- When voltage across the terminals exceeds the breakover voltage, the four out of five layers conduct.
- Name is derived from **DI**ode that can work on **AC**.
- It’s terminals are interchangeable.
- Turn on voltage is around 30 V.
- While conducting, voltage drop across it is around 3 V

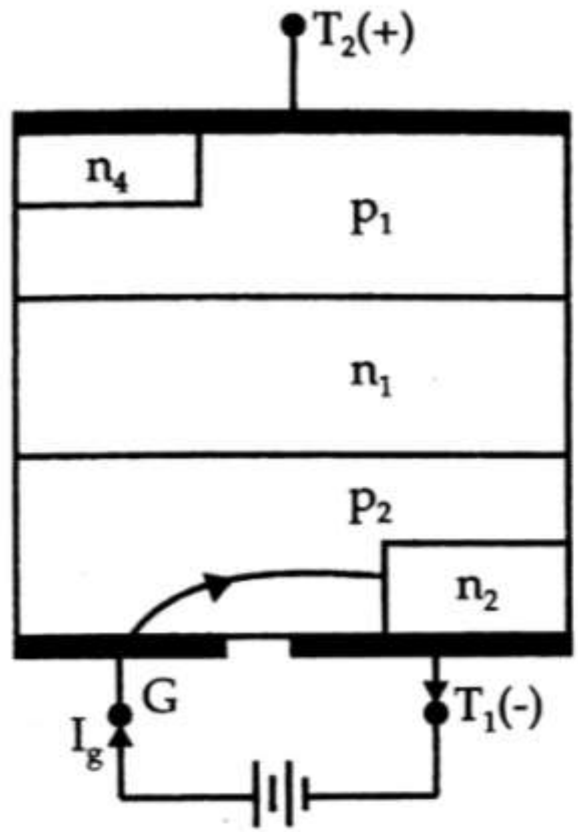
TRIAC



(a) (b)

Modes of Operation

T_2 Positive and Gate Positive

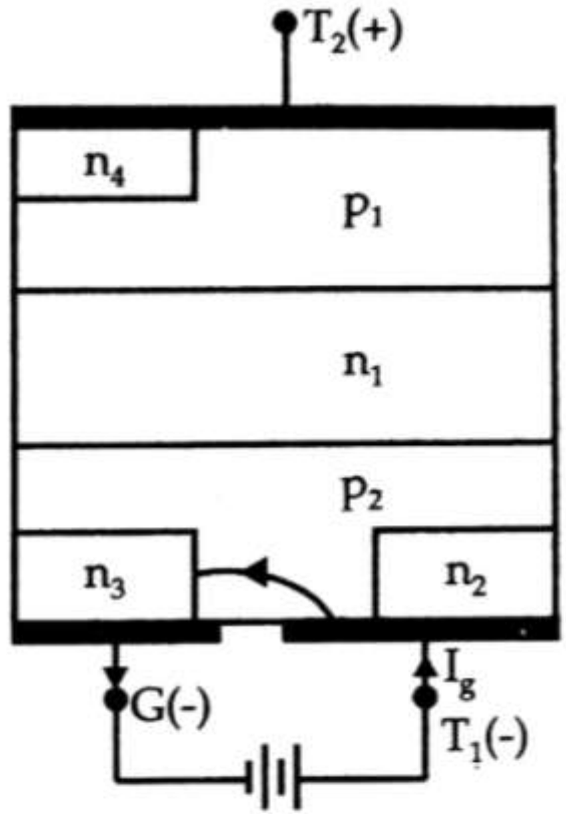


(a)

T_2 Positive and Gate Positive

- Junction $p_1 - n_1$ and $p_2 - n_2$ are forward biased.
- Junction $n_1 - p_2$ is reverse biased.
- Gate current injects sufficient carriers in p_2 layer and Junction $n_1 - p_2$ breaks down.
- Device is more sensitive in this mode.

T_2 Positive and Gate Negative



(b)

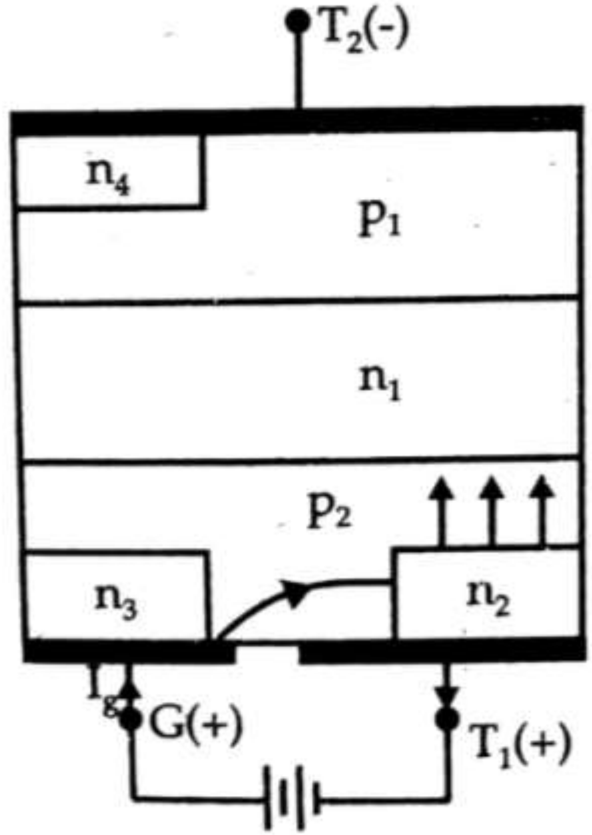
T_2 Positive and Gate Negative

- Junction p_1 n_1 and p_2 n_2 are forward biased.
- Junction n_1 p_2 is reverse biased.
- Gate current flows through p_2 n_3 junction.
- Initially TRIAC current flows through p_1 n_1 p_2 n_3.
- Due to conduction of p_1 n_1 p_2 n_3, the potential of left side of the layer p_2 rises towards anode potential of T_2.

T_2 Positive and Gate Negative

- Potential gradient exists between across the layer $p_{2.}$
- Left side being at higher potential, the current is established in p_2 layer from left to right.
- p_1 n_1 p_2 n_2 start conducting like normal SCR.
- p_1 n_1 p_2 n_3 may be regarded as pilot SCR.
- Device is less sensitive in this mode, so require more gate current.

T_2 Negative and Gate Positive

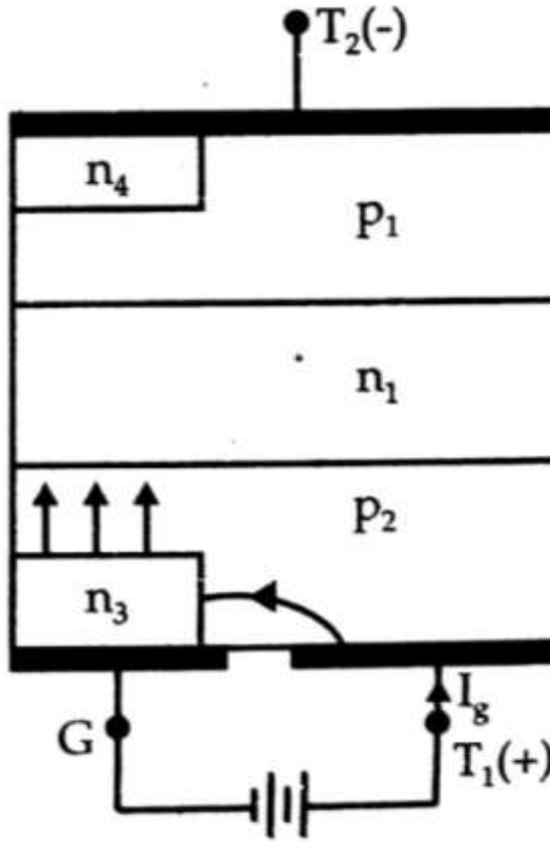


(c)

T_2 Negative and Gate Positive

- Gate current forward biases the p_2 n_2 junction.
- Layer n_2 injects electrons in p_2 layer.
- Reverse biased junction n_1 p_1 breaks down.
- P_2 n_1 p_1 n_4 is completely turned on.
- As the TRIAC is turned on by remote gate n_2 the device is less sensitive.

T2 and Gate is Negative



(d)

T2 and Gate is Negative

- n_3 acts as remote gate.
- Gate current flows from p_2 to n_3 as in normal Thyristor.
- Reverse biased junction n_1 p_1 breaks down.
- Structure p_2 n_1 p_1 n_4 is turned on.
- Device is more sensitive.

Quadracs

- Quadracs are a special type of thyristor which combines a "diac" and a "triac" in a single package.
- The diac is the triggering device for the triac.
- Quadracs eliminate the need to buy and assemble discrete parts.
- Quadracs are used in lighting control, speed control, and temperature modulation control applications.

Heat Sinks

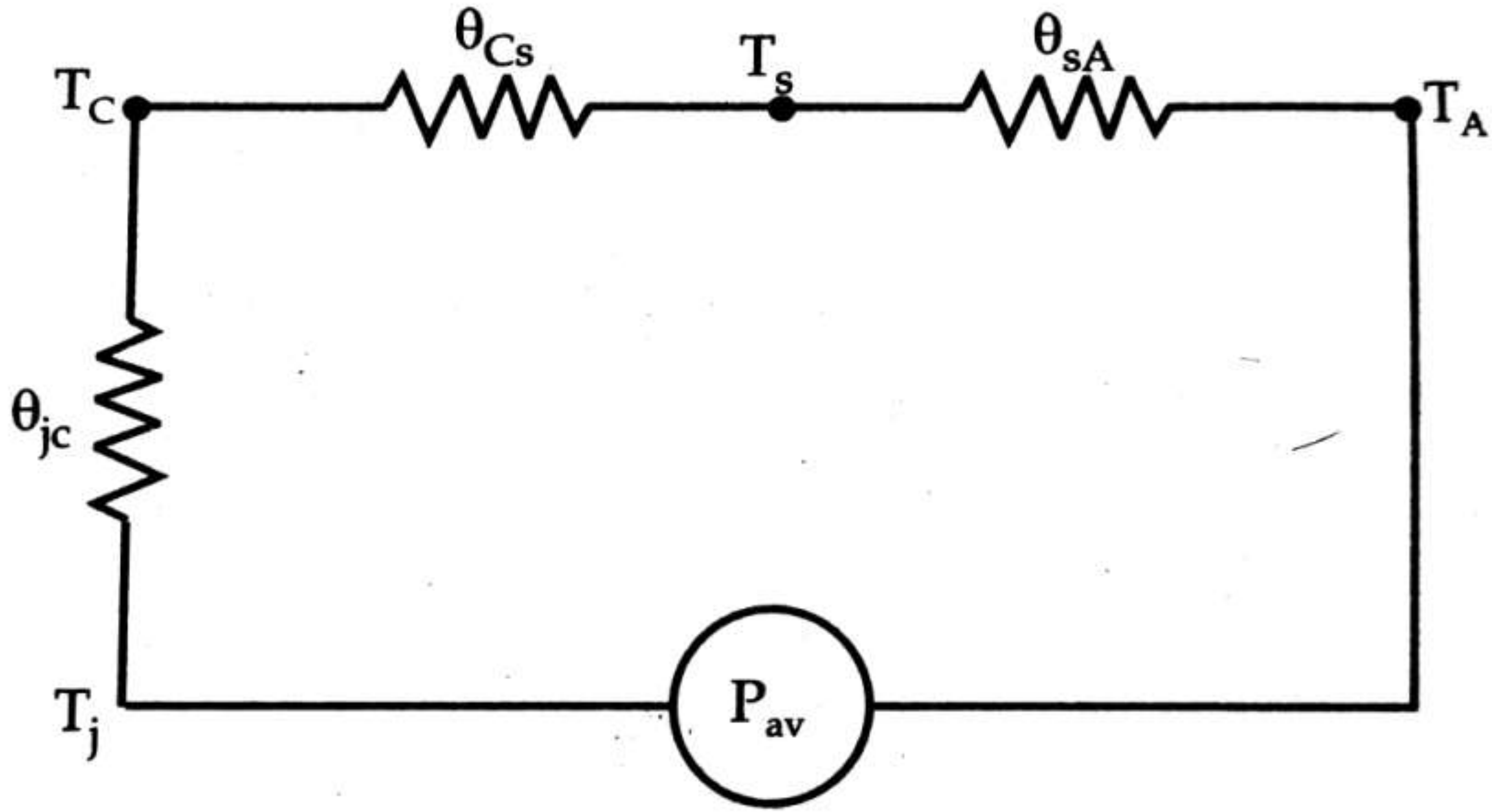
- Small voltage drop exists at Thyristor Junctions.
- With flow of current, heat is developed at junctions.
- Junction temperature may increase beyond permissible limits.
- It may damage the Thyristor.
- To keep junction temperature within limits, Thyristor are mounted on Heat Sinks.

Thermal Ohm's Law

$$P21 = \frac{T2 - T1}{\theta 21}$$

- Θ_{21} = Thermal Resistance between point 2 and 1
- P_{21} = Heat flow from point 2 and 1, W
- T_2 = Temperature of point 2, ^{o}C
- T_1 = Temperature of point 1, ^{o}C

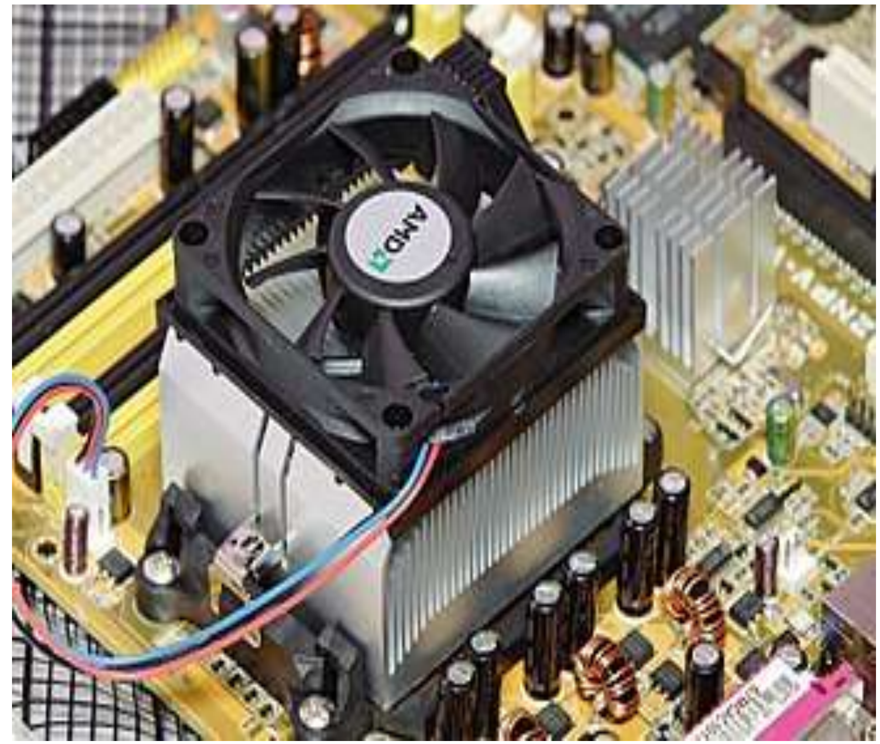
Thermal Equivalent Circuit

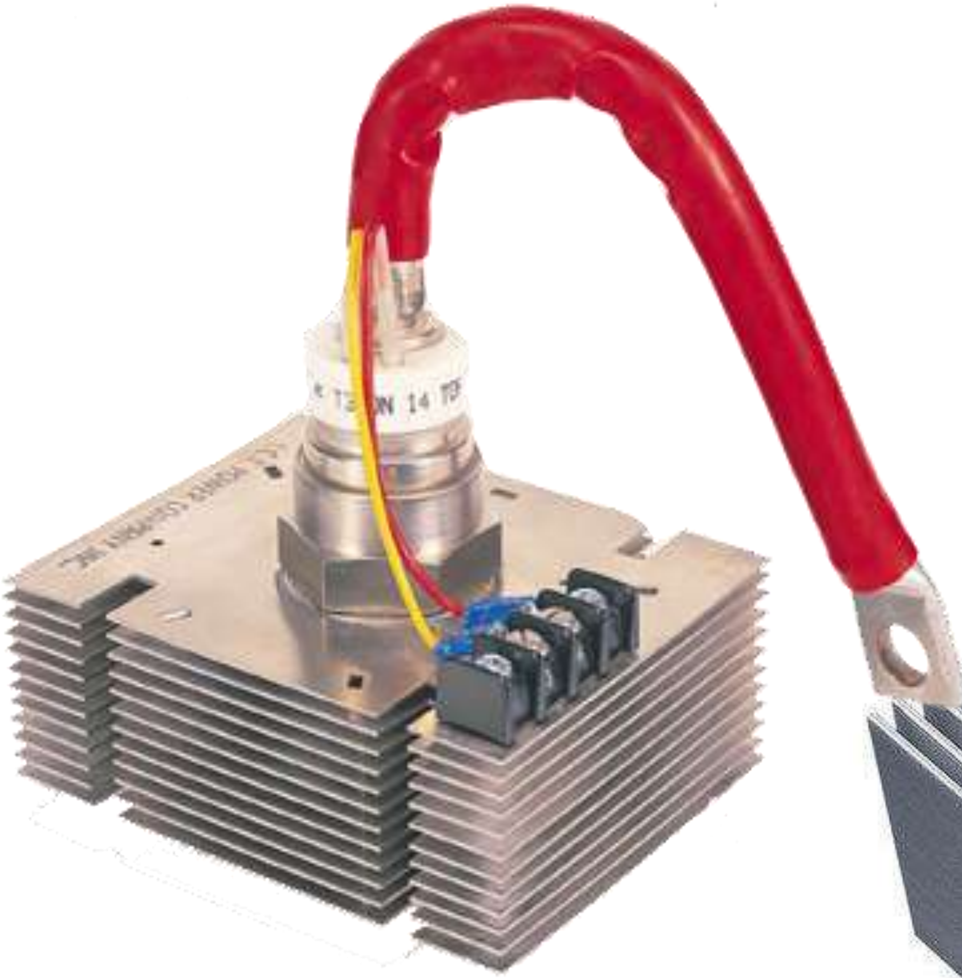


Thermal Equivalent Circuit

- P_{av} : average power loss in the device
- T_j : Temperature of Junction
- T_c : Temperature of Case
- T_s : Temperature of Sink
- T_a : Ambient Temperature
- Θ_{jc} : Thermal Resistance from junction to case
- Θ_{cs} : Thermal Resistance from case to sink
- Θ_{sA} : Thermal Resistance from sink to atmosphere

- Normally Θ_{jc} and Θ_{cs} are specified by the manufacturer.
- Once P_{av} is known, the required Θ_{sA} is calculated for known T_{a}.
- Next step is to choose a heat sink and its size which would meet the thermal resistance requirement.
- Copper and Aluminum heat sinks are preffered.


AMD



Thyristor Tiggering

Forward Voltage Triggering

- When anode – cathode increases beyond the forward break over voltage V_{BO}, reverse biased junction J_2 breaks down due to Avalache breakdown.
- Anode current is limited by load impedance only.

Gate Triggering

- Simple, reliable and efficient method to turn on the SCR and is mostly used.
- Positive gate voltage between gate and cathode is applied.
- Charges are injected in to inner p layer
- The voltage at which forward break over occurs, is reduced.
- Higher the gate current, lower is the forward break over voltage.
- Typical gate current is 20 to 200 mA.

Gate Triggering

- With positive gate current, p layer is flooded with electrons from cathode as n layer is heavily doped as compared to gate p layer.
- Some of these electrons reach junction J2.
- Due to this, width of depletion layer near junction J2 is reduced and it breaks down at lower voltage.
- Reverse biased junction J2 no longer exists.
- If gate current is removed, anode to cathode current remains unaffected.

dv/dt Triggering

- Reverse biased junction J_2 has characteristics similar to capacitor due to charges existing across the junction.
- If forward voltage is suddenly applied, the charging current through junction capacitance may turn on the SCR.

$$ic = \frac{dQ}{dt} = C\frac{dv}{dt}$$

dv/dt Triggering

- If rate of rise of forward voltage dv/dt is high, the charging current i_c would be more.
- This charging current plays the role of gate current.
- It may turn on the SCR even though gate signal is zero, at lower anode voltages.

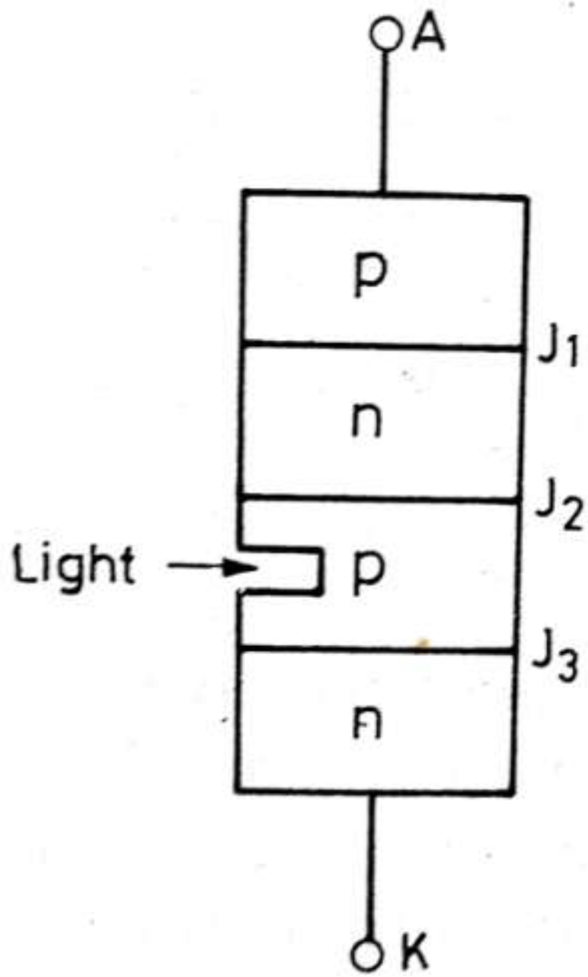
Temperature Triggering

- Applied voltage, associated with leakage current raises the temperature of the junction J_2.
- With increase in temperature, width of depletion layer decreases.
- This further leads to more leakage current and therefore more junction temperature.

Temperature Triggering

- With the cumulative process, at some high temperature (Within the safe limits), depletion layer of reverse biased junction vanishes and device gets turned on.

Light Triggering

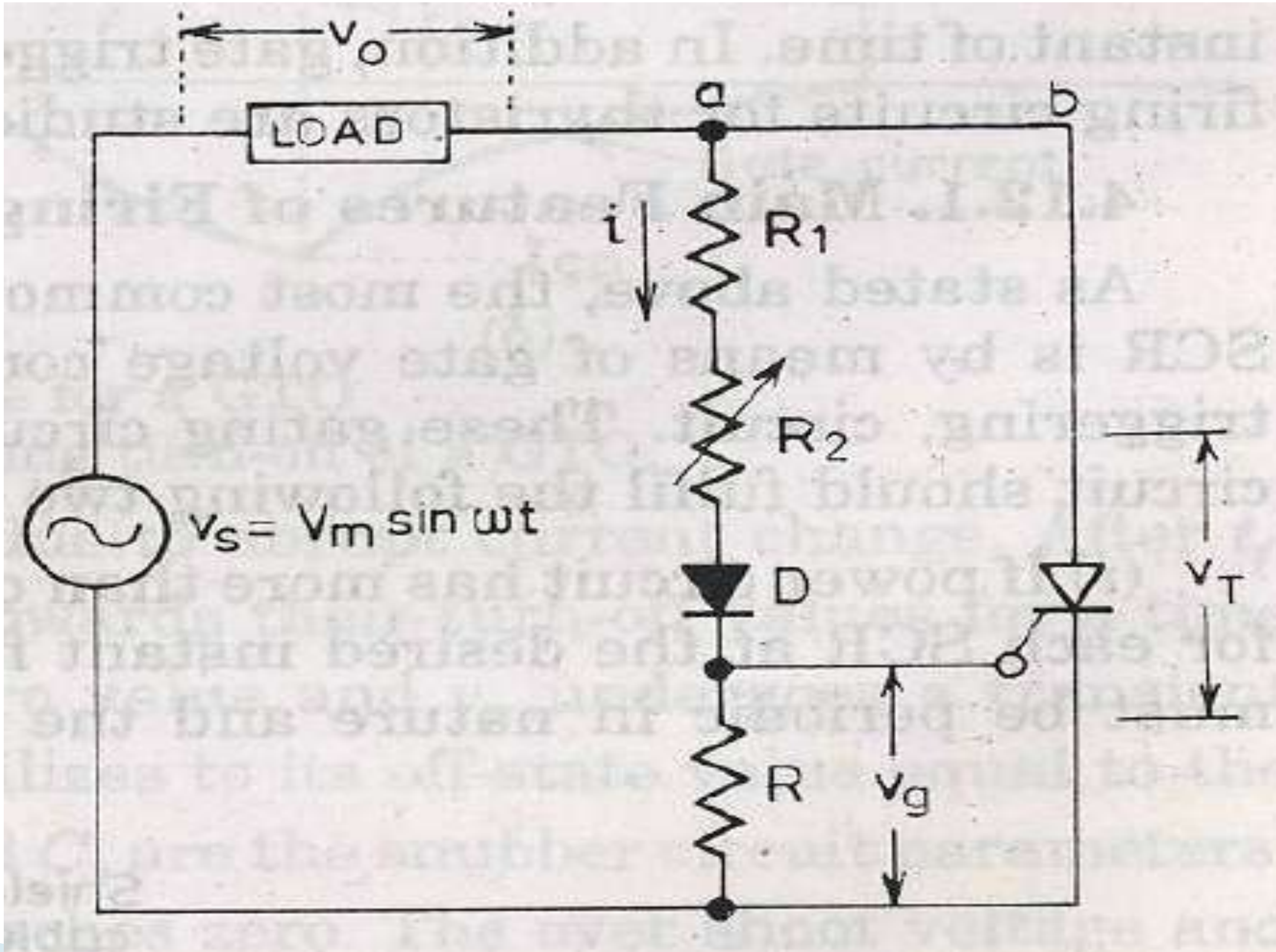


Light Triggering

- Light triggered SCRs has a recess made in the inner p-layer.
- When this recess is irradiated, free charge carriers are generated.
- With sufficient light at recess, the forward biased SCR is turned on.
- Such a thyristor is called Light Activated SCR (LASCR).
- LASCR may be triggered with a light source or with gate signal.

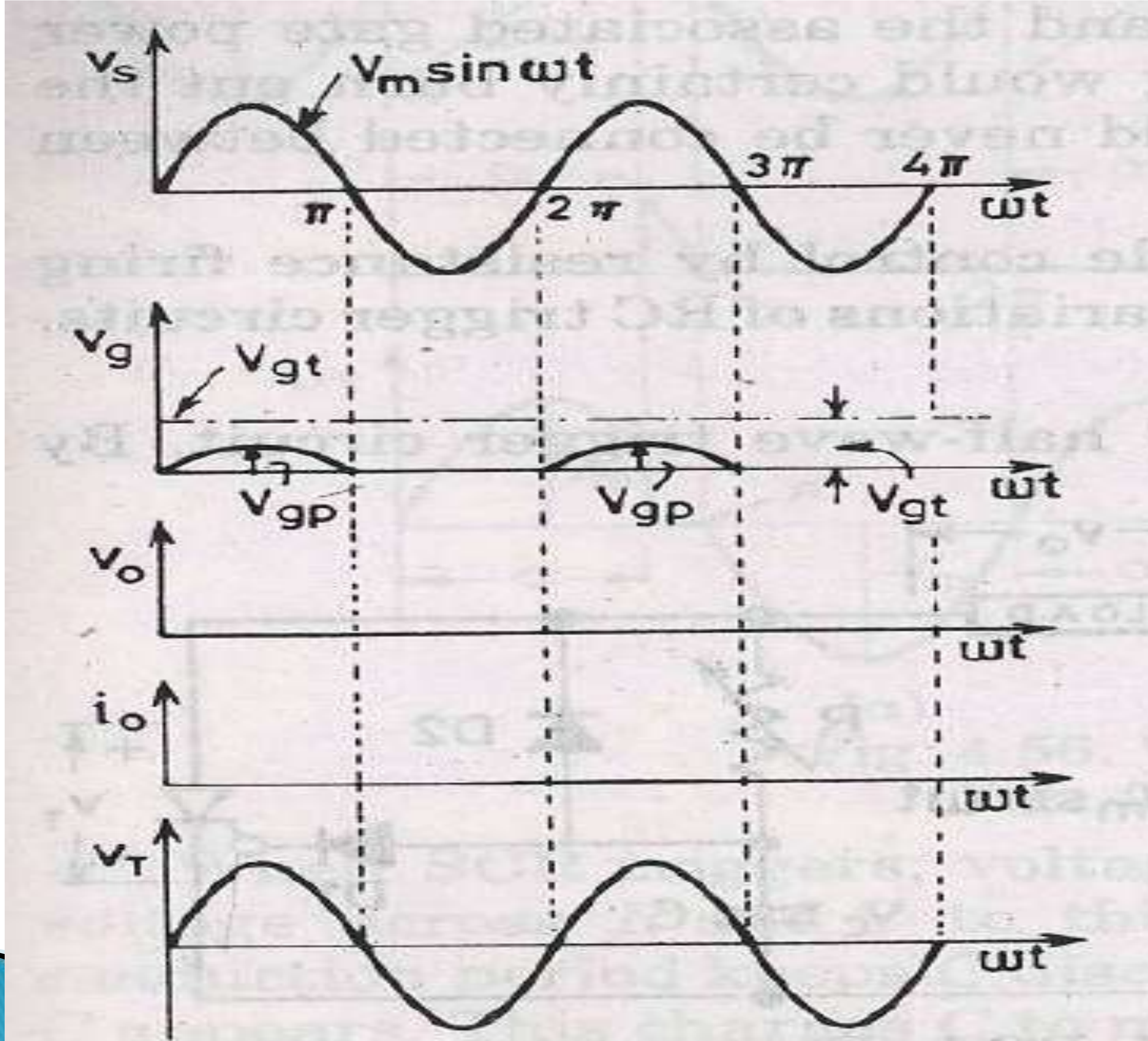
Triggering Circuits

Resistance Triggering

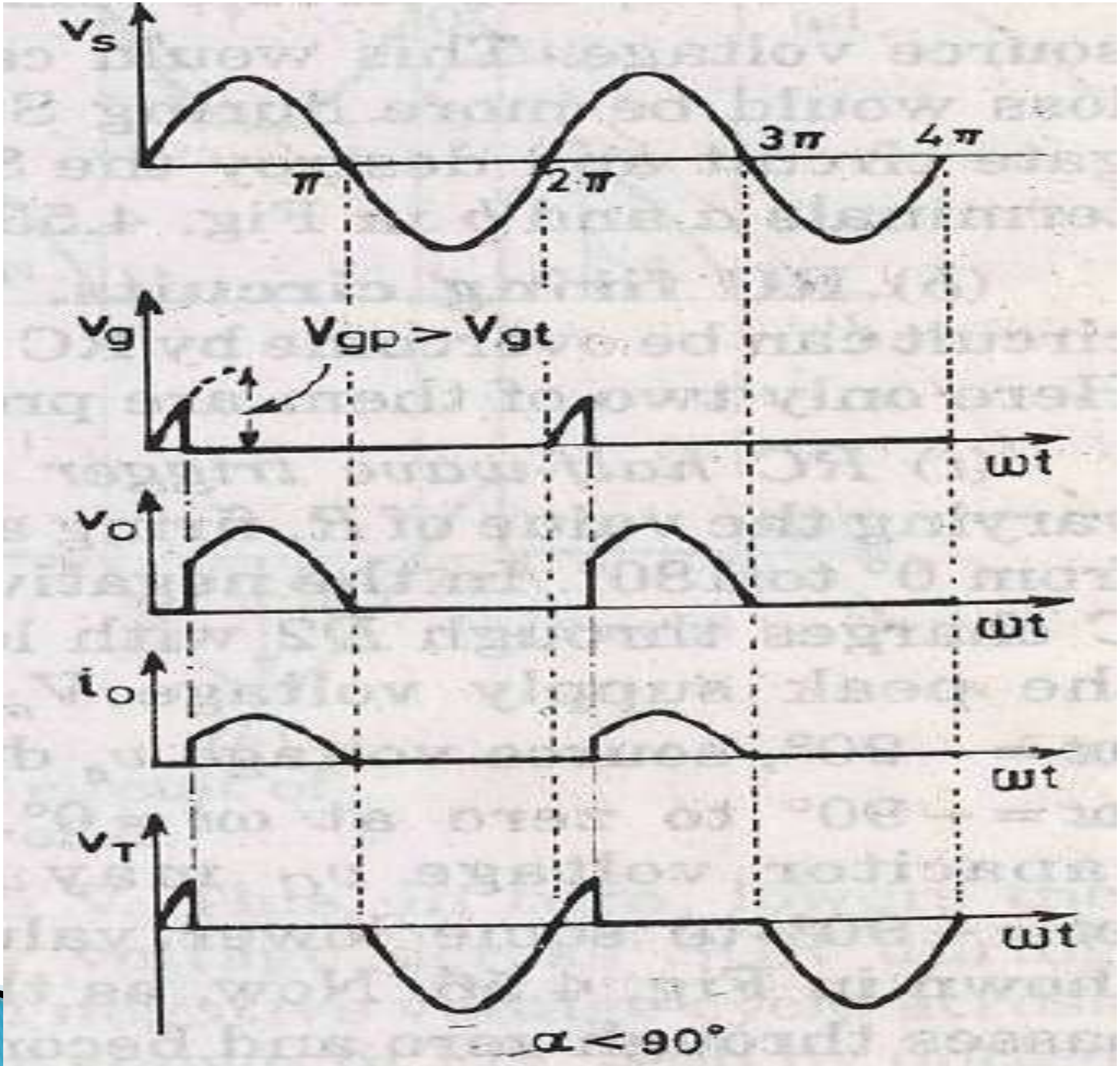


Resistance Triggering

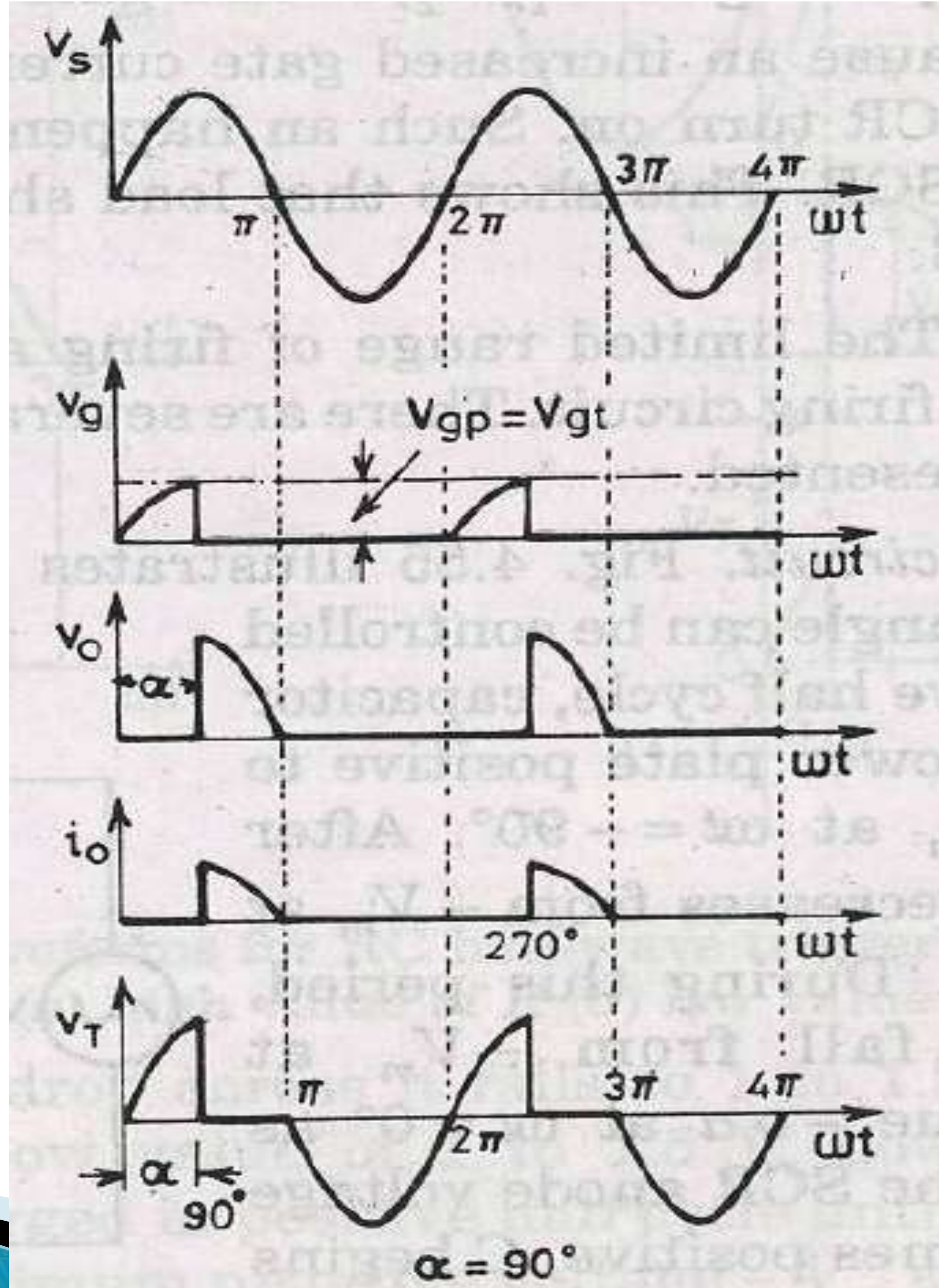
- Simplest and most economical.
- Limited firing angle control (0–90°).
- The function of R_1 is to limit the gate current to safe value, as R_2 is varied.
- R_1 should be greater than or equal to V_m/I_{gm}. Where V_m is maximum source voltage and I_{gm} is maximum permissible gate current.



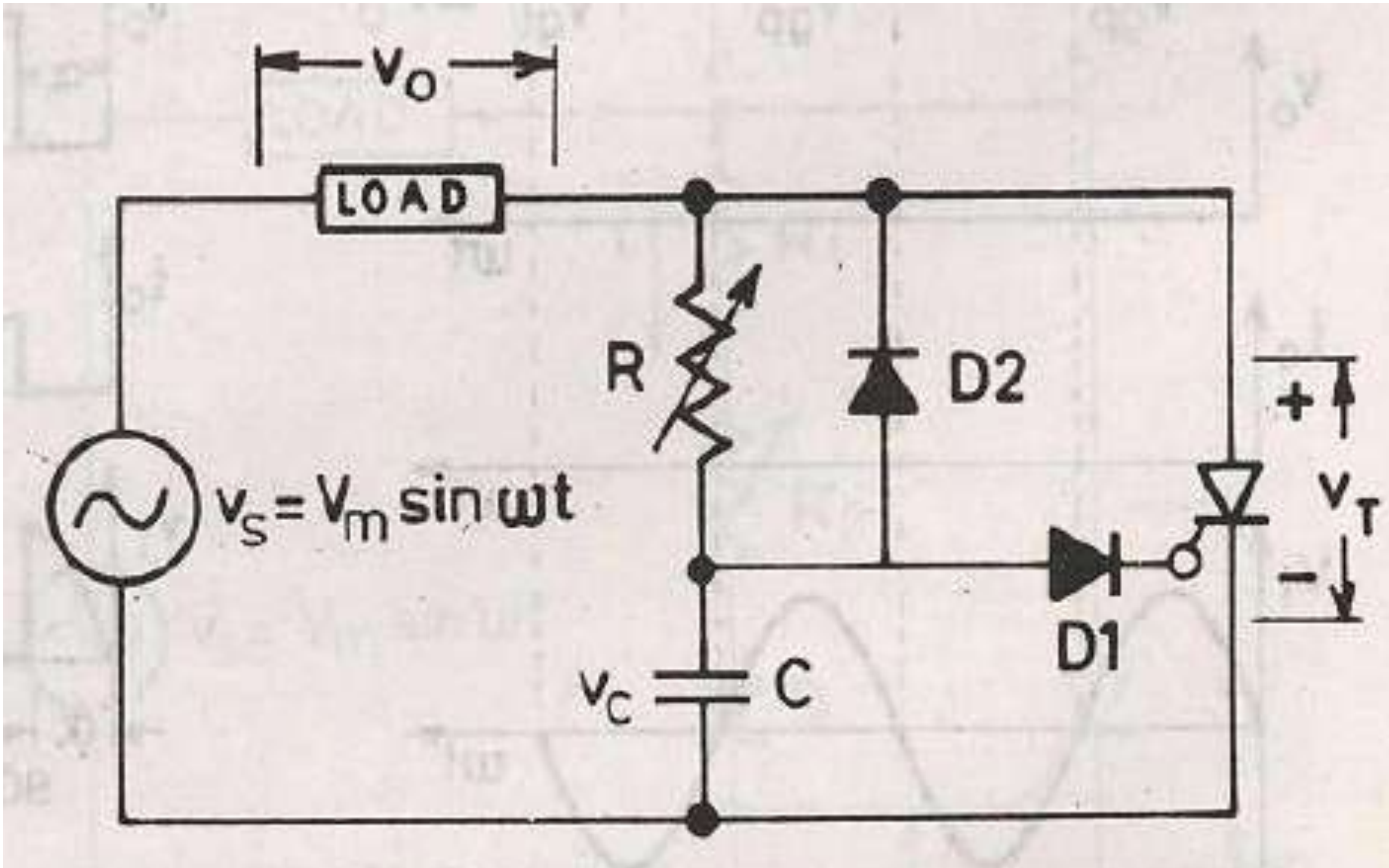
v_s
$V_m \sin \omega t$
π
2π
3π
4π
ωt
v_g
V_{gt}
V_{gp}
V_{gp}
V_{gt}
ωt
v_o
ωt
i_o
ωt
v_T
ωt



v_s
π
2π
3π
4π
v_g
$V_{gp} > V_{gt}$
ωt
v_o
ωt
i_o
ωt
v_T
ωt
$\alpha < 90°$


Vs
π
2π
3π
4π
ωt
Vg
Vgp = Vgt
ωt
Vo
α
ωt
io
270°
ωt
vT
π
2π
3π
4π
ωt
α
90°
α = 90°

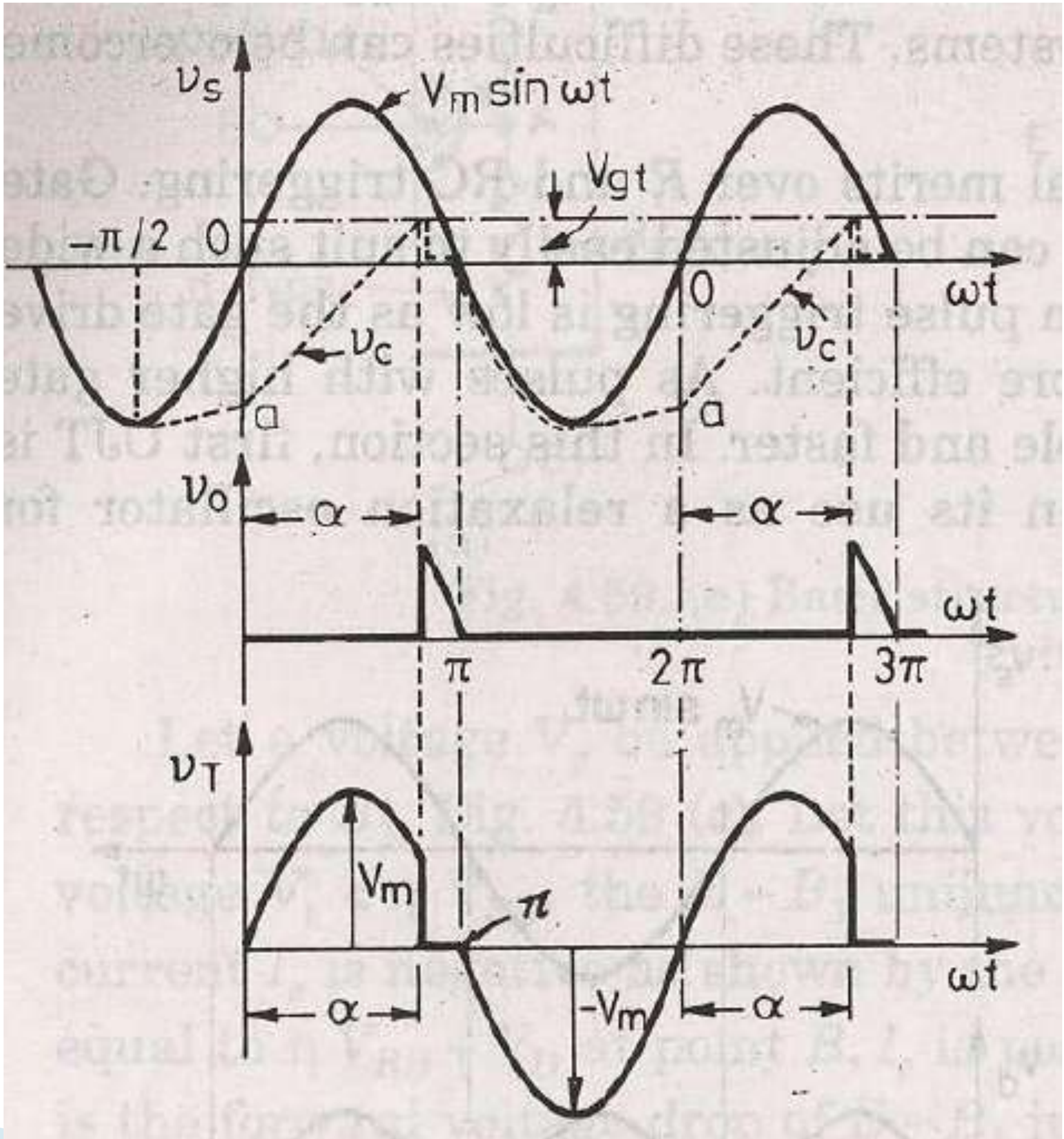
RC Half Wave Triggering Circuit



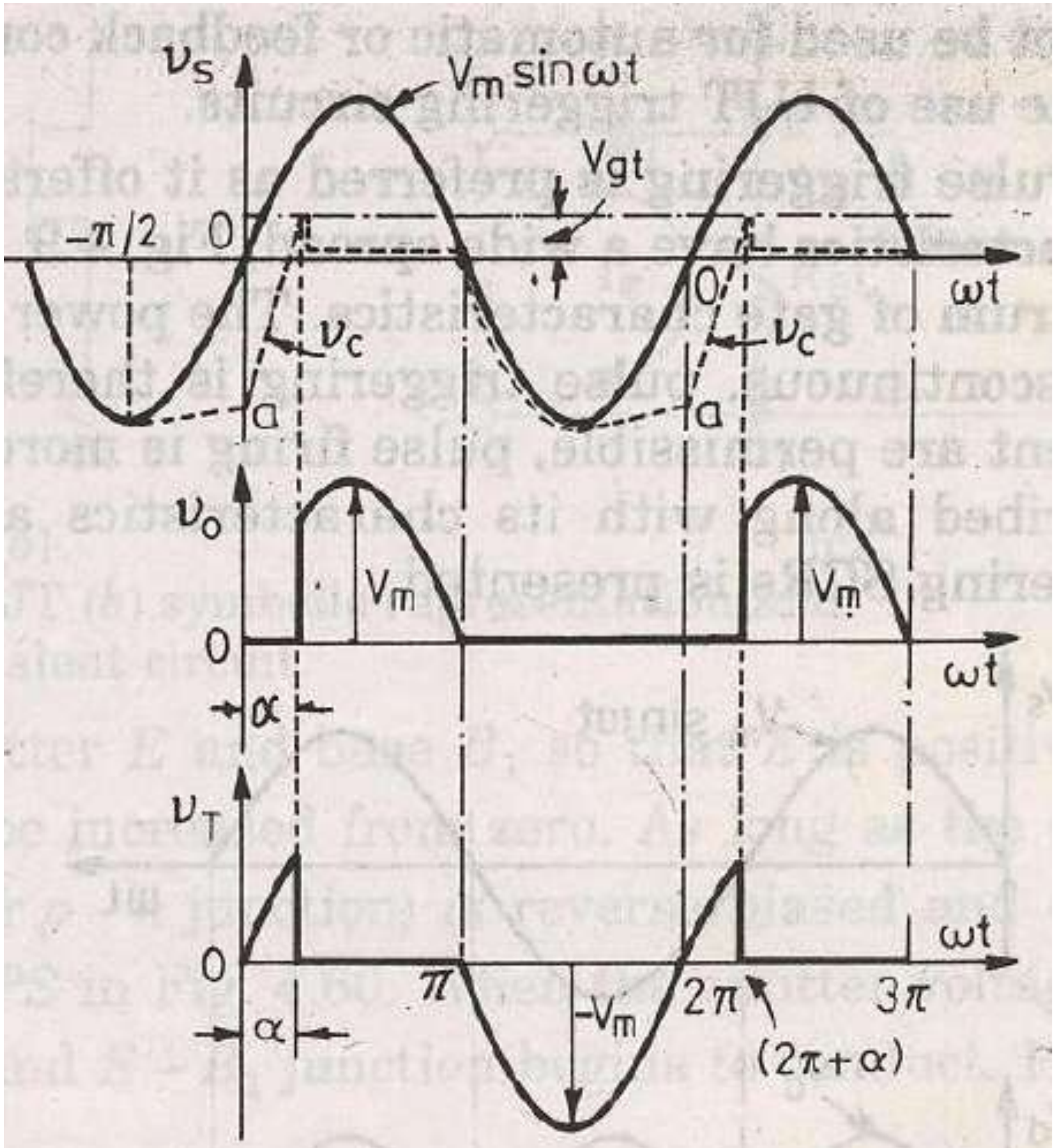
RC Half Wave Triggering Circuit

- By varying the value of R, firing angle can be controlled from 0 – 180°.
- In negative half, the capacitor charges through D2 with lower plate positive to voltage V_m.
- In positive half, capacitor C begins to charge through resistance R.
- When capacitor voltage reaches V_{gt}, SCR is fired.
- $[V_c = V.(1 - e^{(-t/RC)})]$

- Diode D_1 is used to prevent the breakdown of cathode to gate junction through D_2, during negative half cycle.

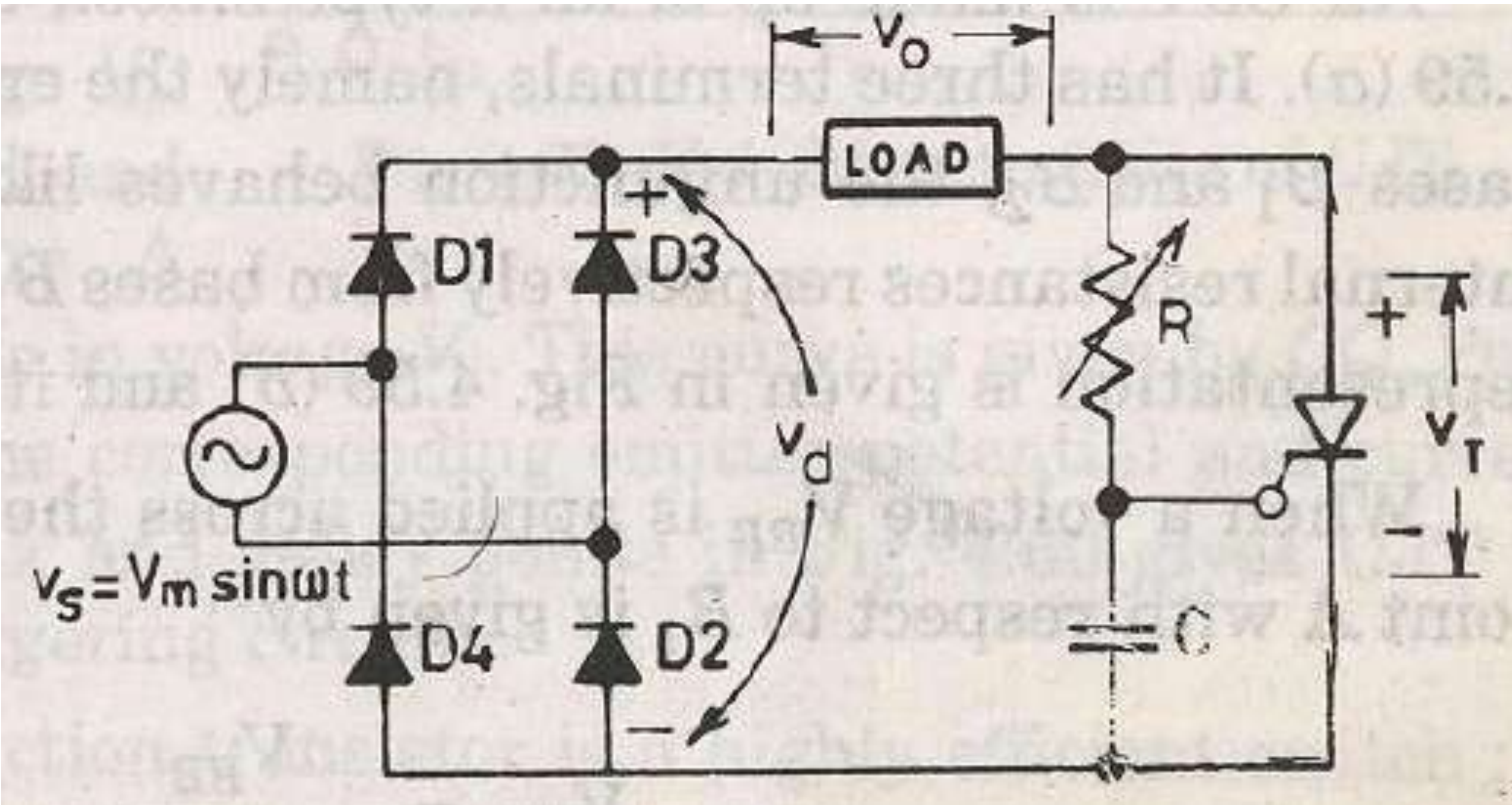


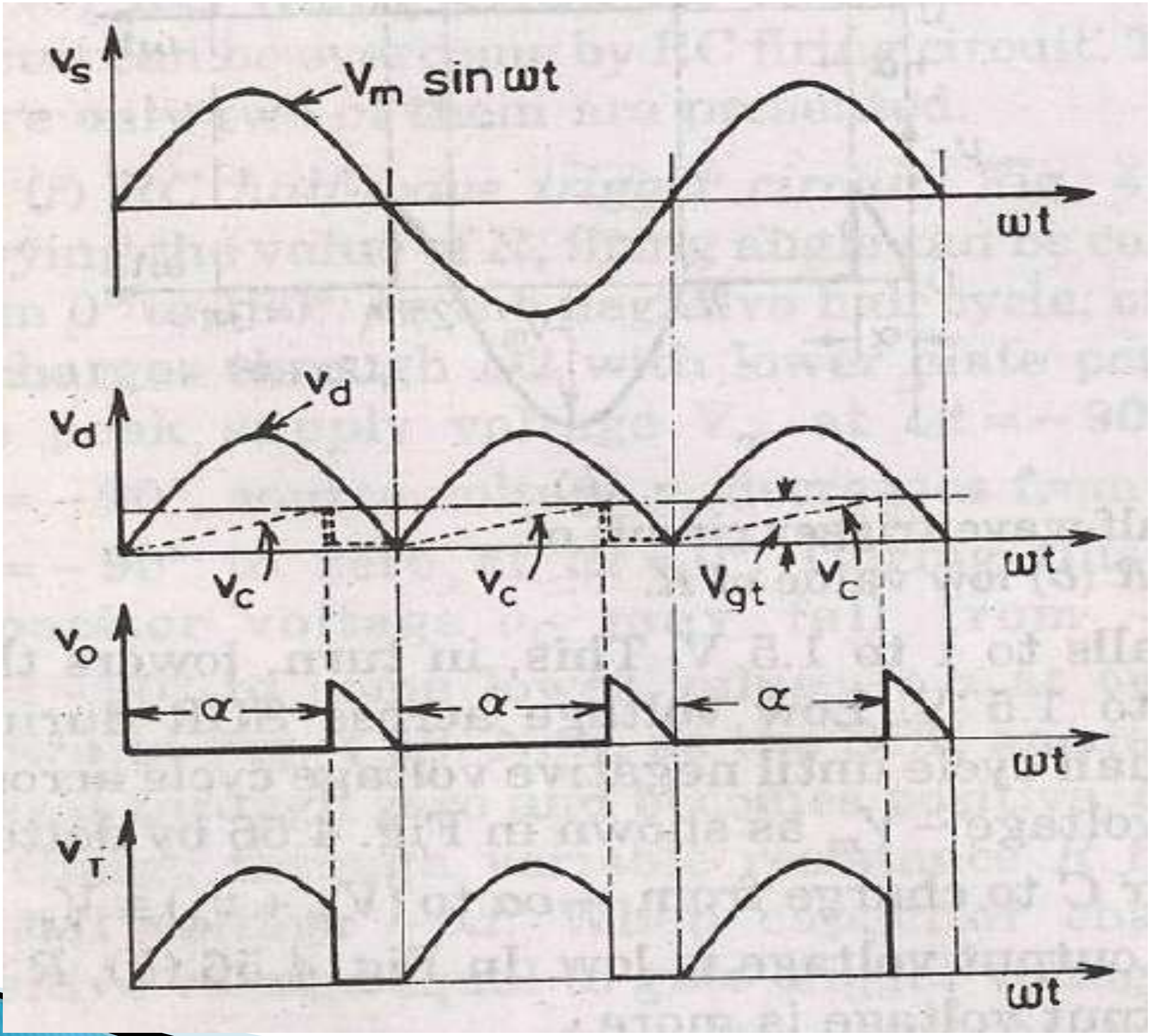
v_s
$V_m \sin \omega t$
V_{gt}
$-\pi/2$
0
0
ωt
v_c
v_c
a
a
v_o
α
α
ωt
π
2π
3π
v_T
V_m
π
$-V_m$
α
α
ωt



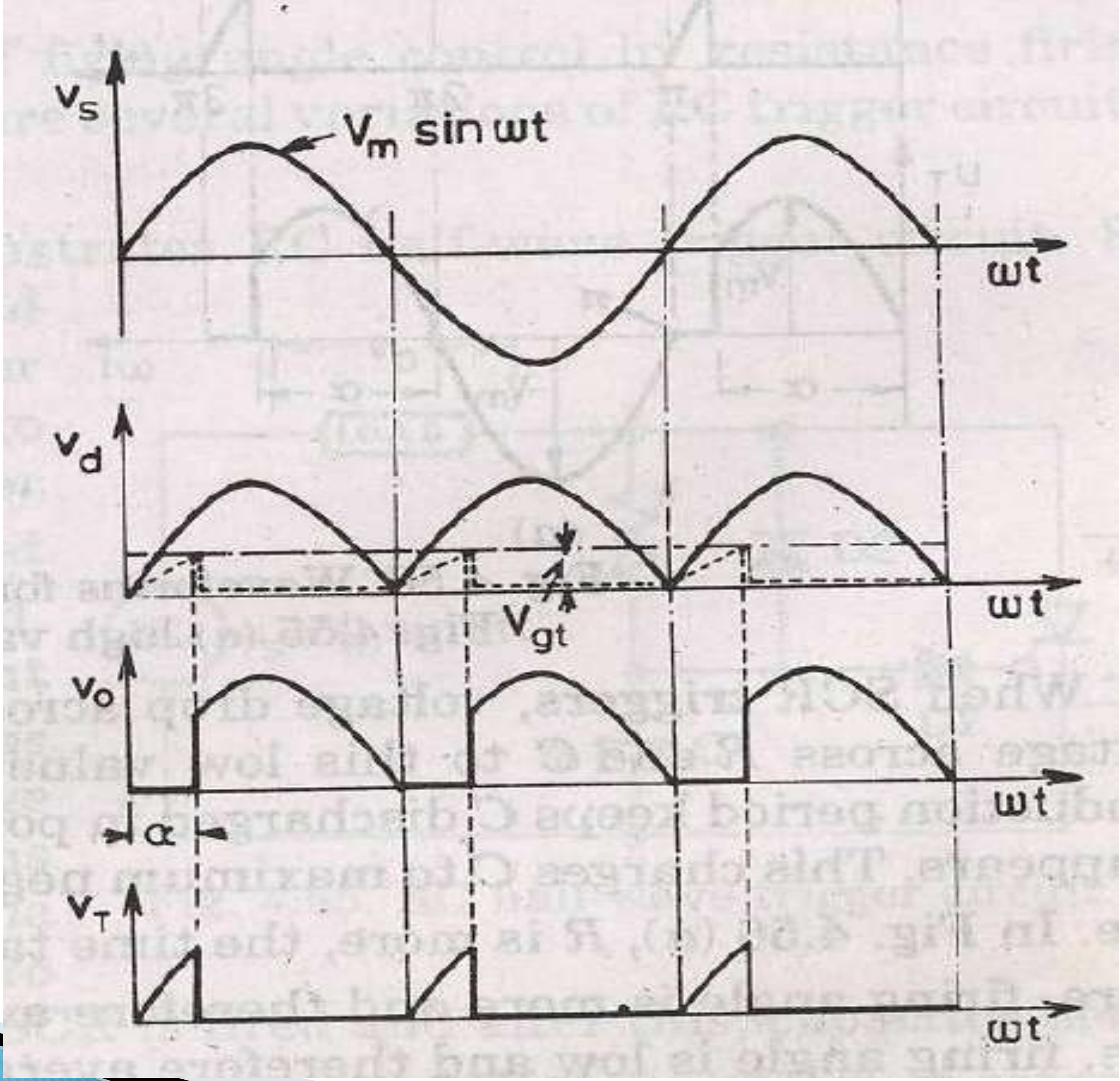
νs
Vm sin ωt
Vgt
−π/2
0
ωt
νc
a
νo
Vm
0
ωt
α
νT
ωt
0
π
−Vm
2π
3π
(2π+α)

RC Full Wave Triggering Circuit



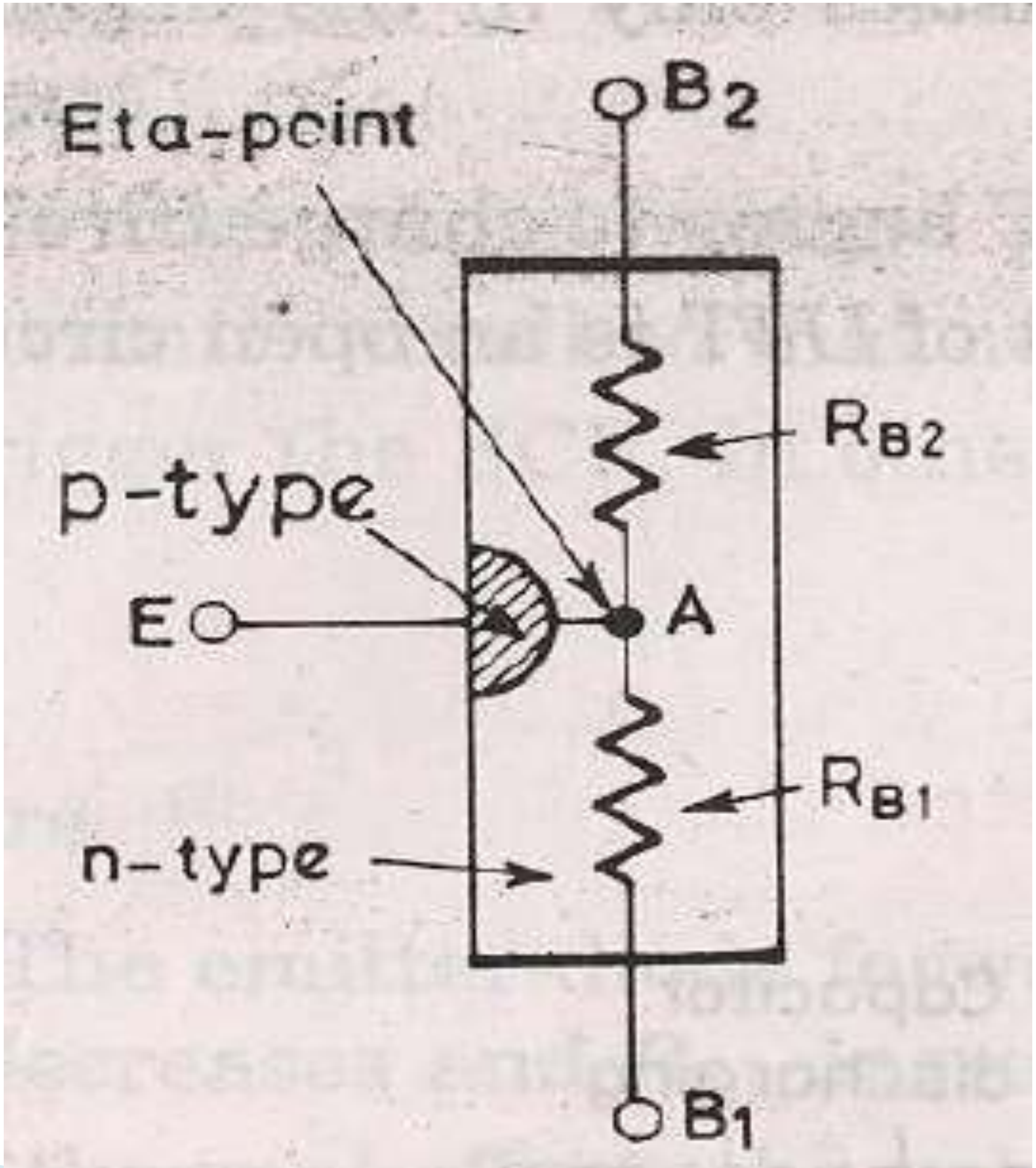


v_s
$V_m \sin\omega t$
ωt
v_d
v_d
v_c
v_c
V_{gt}
v_c
ωt
v_o
α
α
α
ωt
v_T
ωt



v_s
$V_m \sin \omega t$
ωt
v_d
ωt
V_{gt}
v_o
ωt
α
v_T
ωt

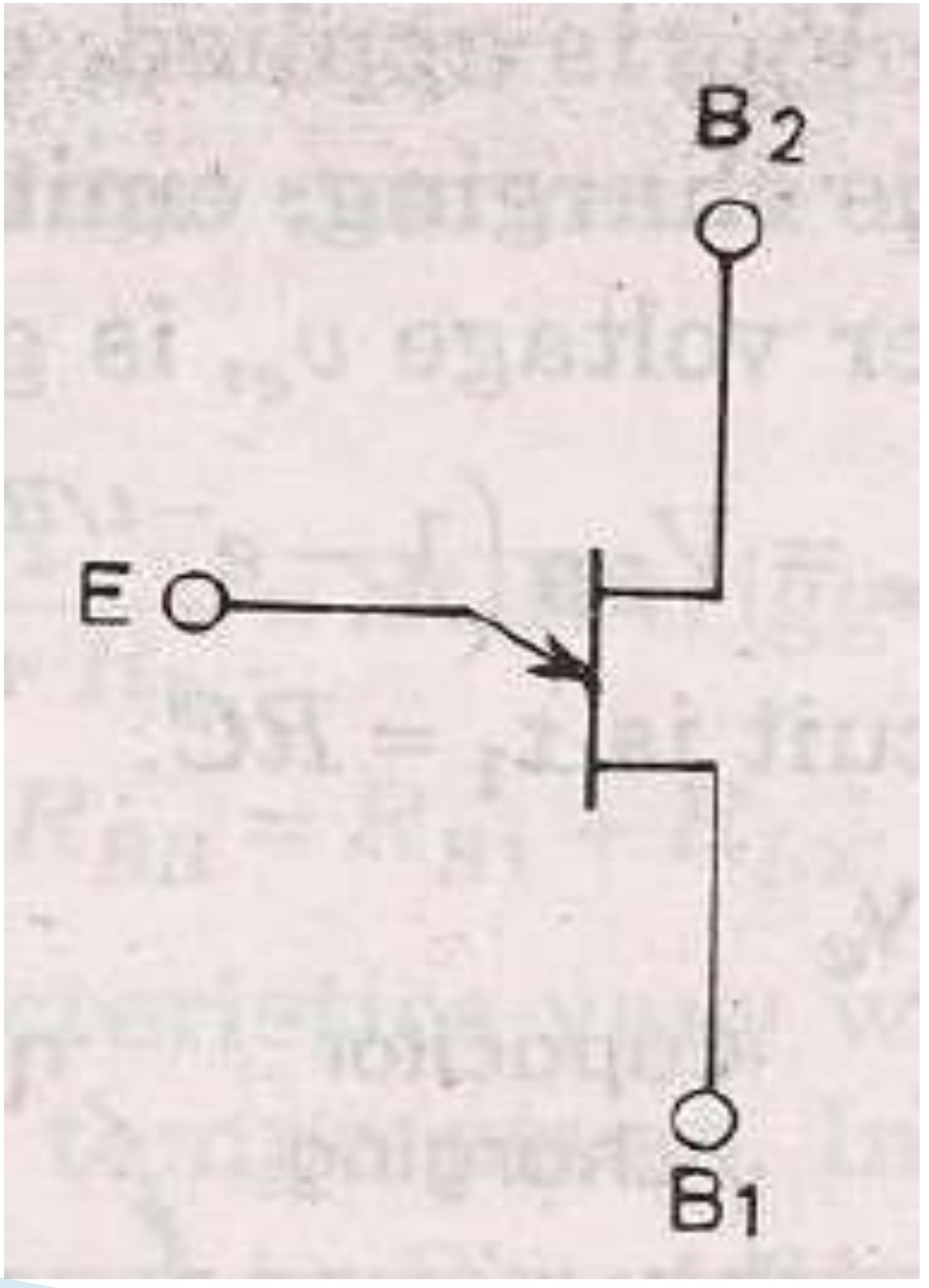
Unijunction Transistor (UJT)

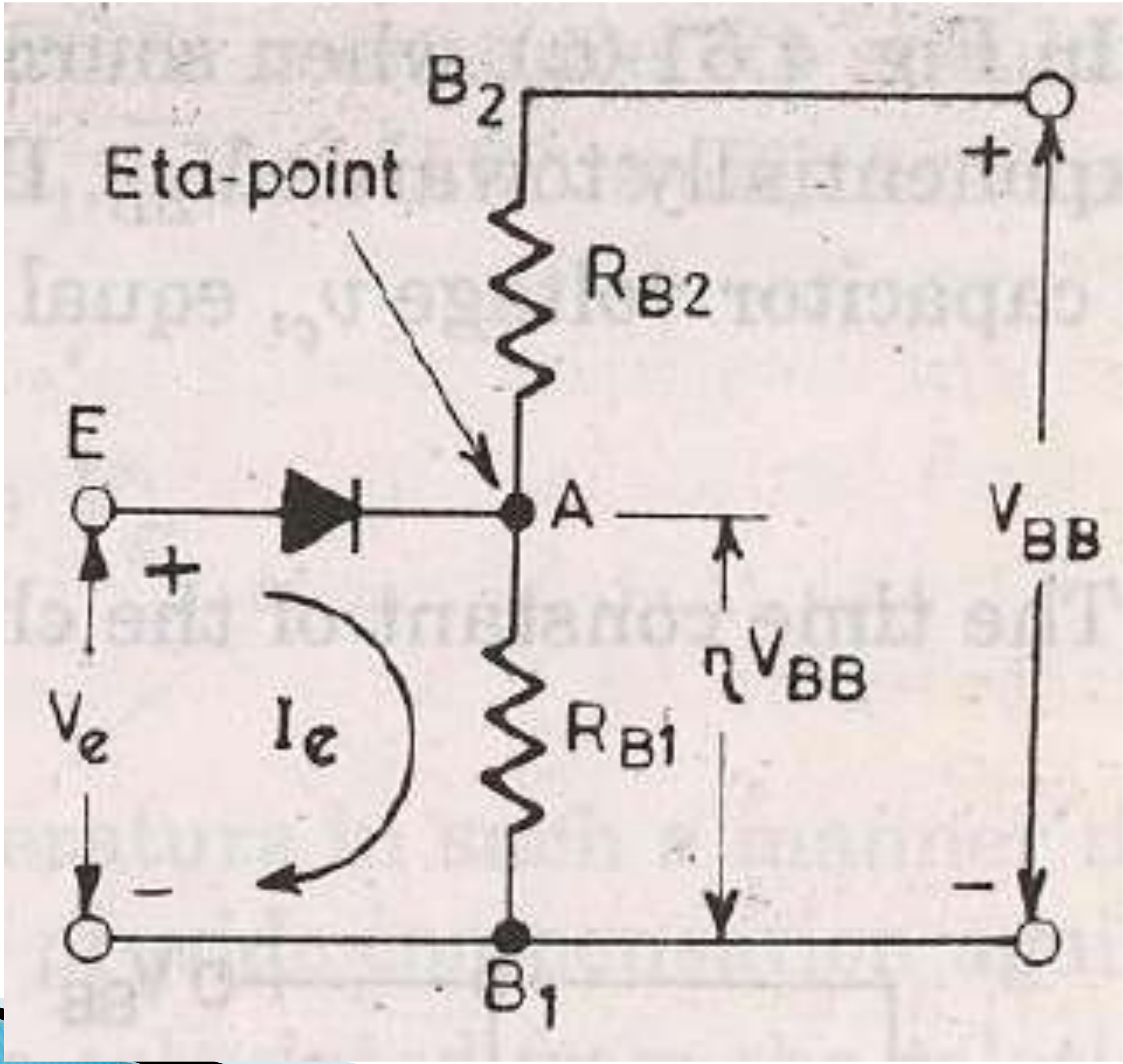

B2
Eta-pcint
R_B2
p-type
E
A
R_B1
n-type
B1

- UJT is made of an n–type silicon base to which p–type emitter is embedded.
- n–type base is lightly doped, whereas p–type emitter is heavily doped.
- Between bases B_1 and B_2, unijunction behaves like an ordinary resistance.
- When V_{BB} is applied between B_1 and B_2

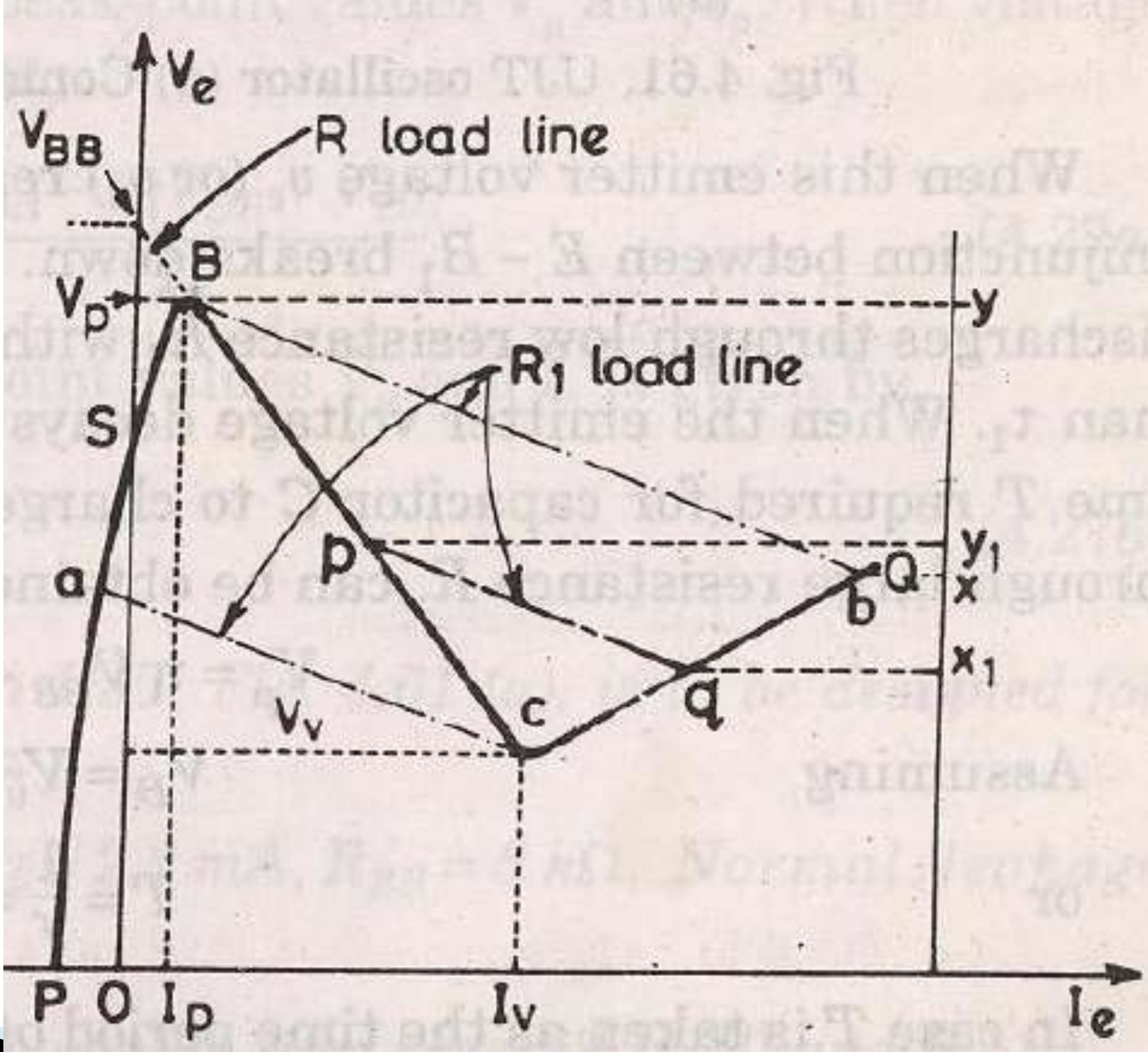
$$V_{AB1} = \frac{V_{BB}}{R_{B1} + R_{B2}} \cdot R_{B1} = \frac{R_{B1}}{R_{B1} + R_{B2}} \cdot V_{BB} = \eta\, V_{BB}$$

- $\eta = \frac{RB1}{RB1+RB2}$ is called the intrinsic standoff ratio.
- Typical values of η are 0.51 to 0.82.
- Inter base resistance $RBB = RB1 + RB2$ is of the order of 5 – 10 KΩ.
- Emitter is nearer to B_2, resistance R_{B2} is less than R_{B1}.


B2
E
B1



B2
Eta-point
RB2
E
A
VBB
+
Ve
Ie
RB1
ηVBB
–
B1



Ve
VBB
R load line
B
Vp
y
R1 load line
S
p
y1
Q
x
a
b
x1
c
q
Vv
P
O
Ip
Iv
Ie

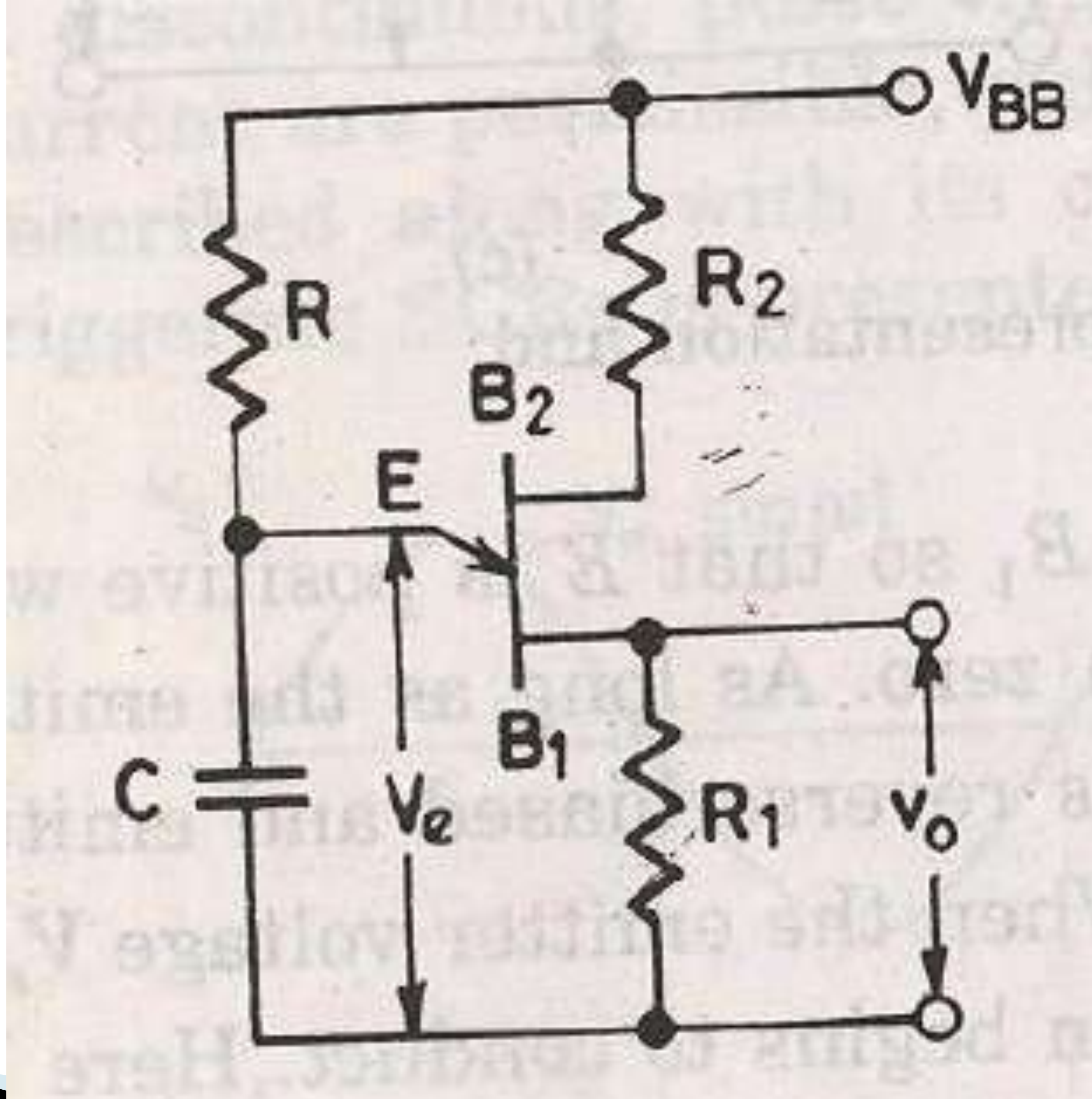
- As long as emitter voltage $V_e < \eta V_{BB,}$ the E–B_1 junction is reverse biased and emitter current I_e is negative.
- At point S, drop across R_E is zero and $I_e = 0$.
- When Ve = $\eta . V_{BB} + V_D$ at point B, E–B_1 junction gets forward biased.
- VD is forward voltage drop across the junction E–B_1 (ususally 0.5V).
- V_p and I_p are called peak voltage and peak current respectively.

- At peak point B, the p–emitter begins to inject holes in to lower base region B_1.
- Resistance R_{B1} suddenly decreases.
- Potential of eta point A drops.
- As V_{EE} is constant, fall of V_e gives rise to more emitter current I_e $(=(V_{EE}-V_e)/R_E)$.
- Increased I_e injects more holes, further reducing R_{B1} and so on.

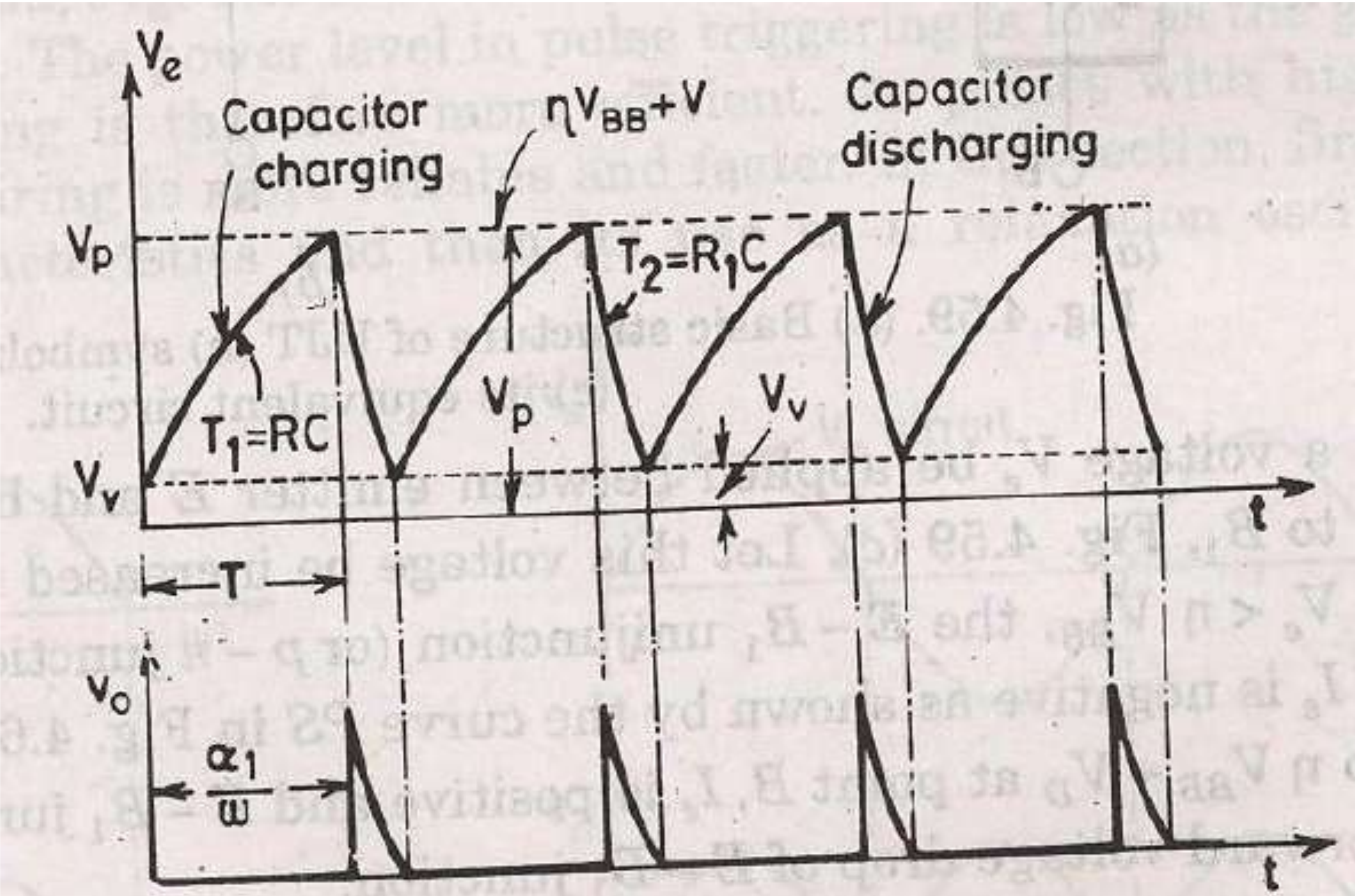
- Regenerative effect continues till R_{B1} has dropped to small value (from about 4KΩ to around 2 to 25Ω).
- Emitter current is limited by external resistance R_E only.
- At valley point (point C), UJT reaches the on state.
- At point C, entire base region is saturated and R_{B1} can not decrease any more.

- Any increase in V_e is accompanied by increase in I_e.
- Between point B and C, V_e Falls and I_e increases.
- UJT, therefore, exhibits negative resistance between point B and C.

UJT Relaxation Oscillator



V_{BB}
R
R_2
B_2
E
B_1
C
V_e
R_1
v_o

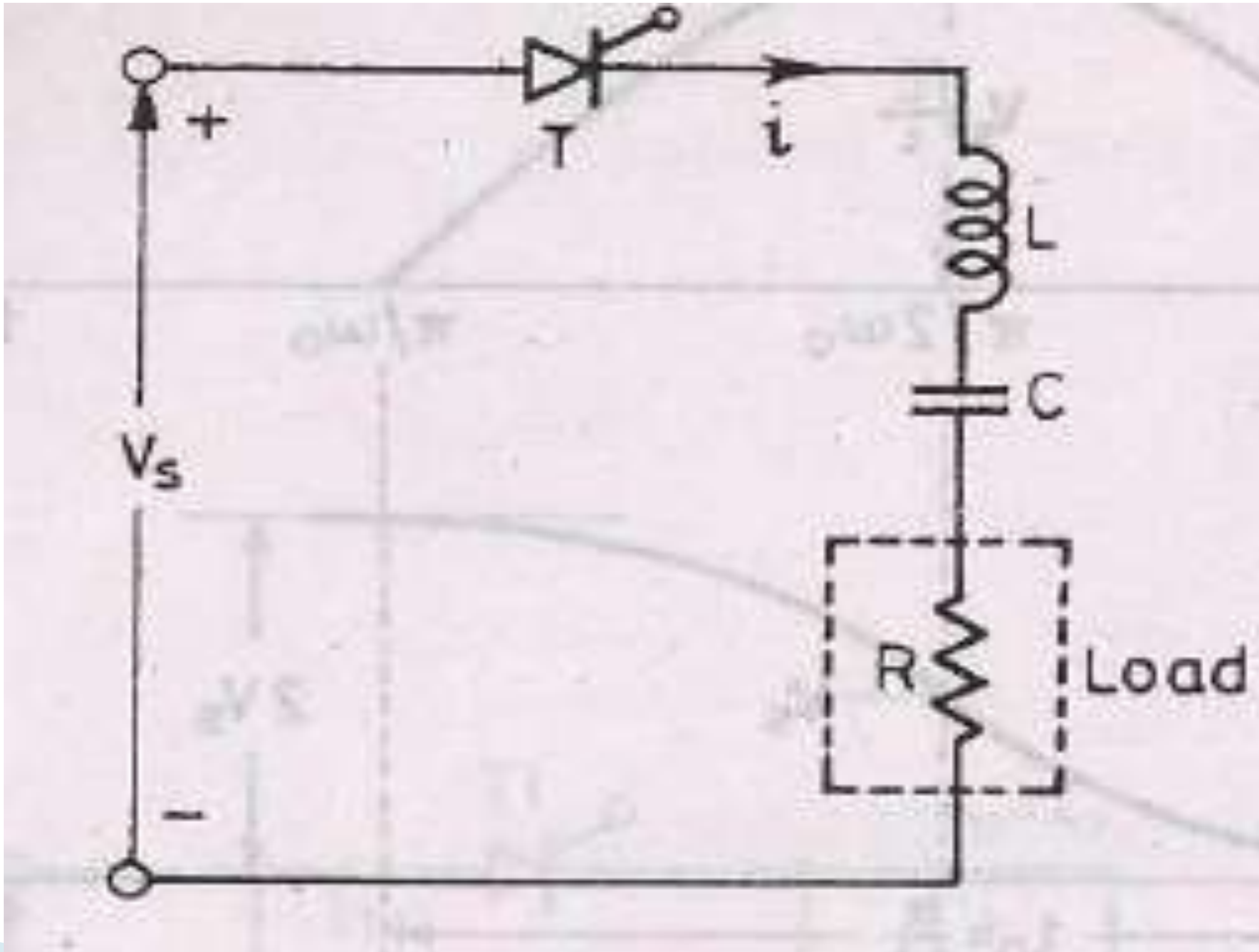


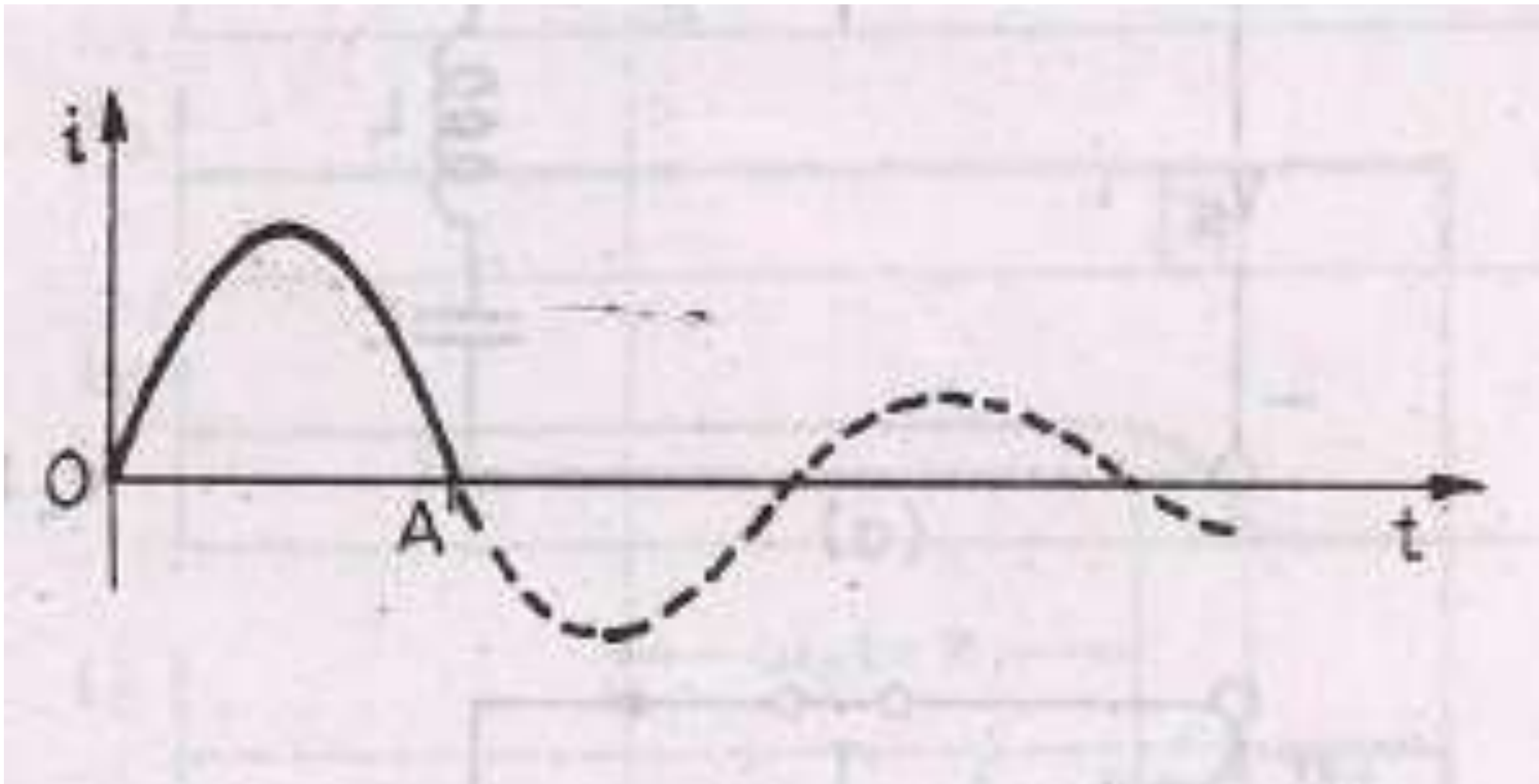
Ve
Capacitor
charging
ηVBB+V
Capacitor
discharging
Vp
T2=R1C
T1=RC
Vp
Vv
Vv
t
T
vo
α1
ω
t

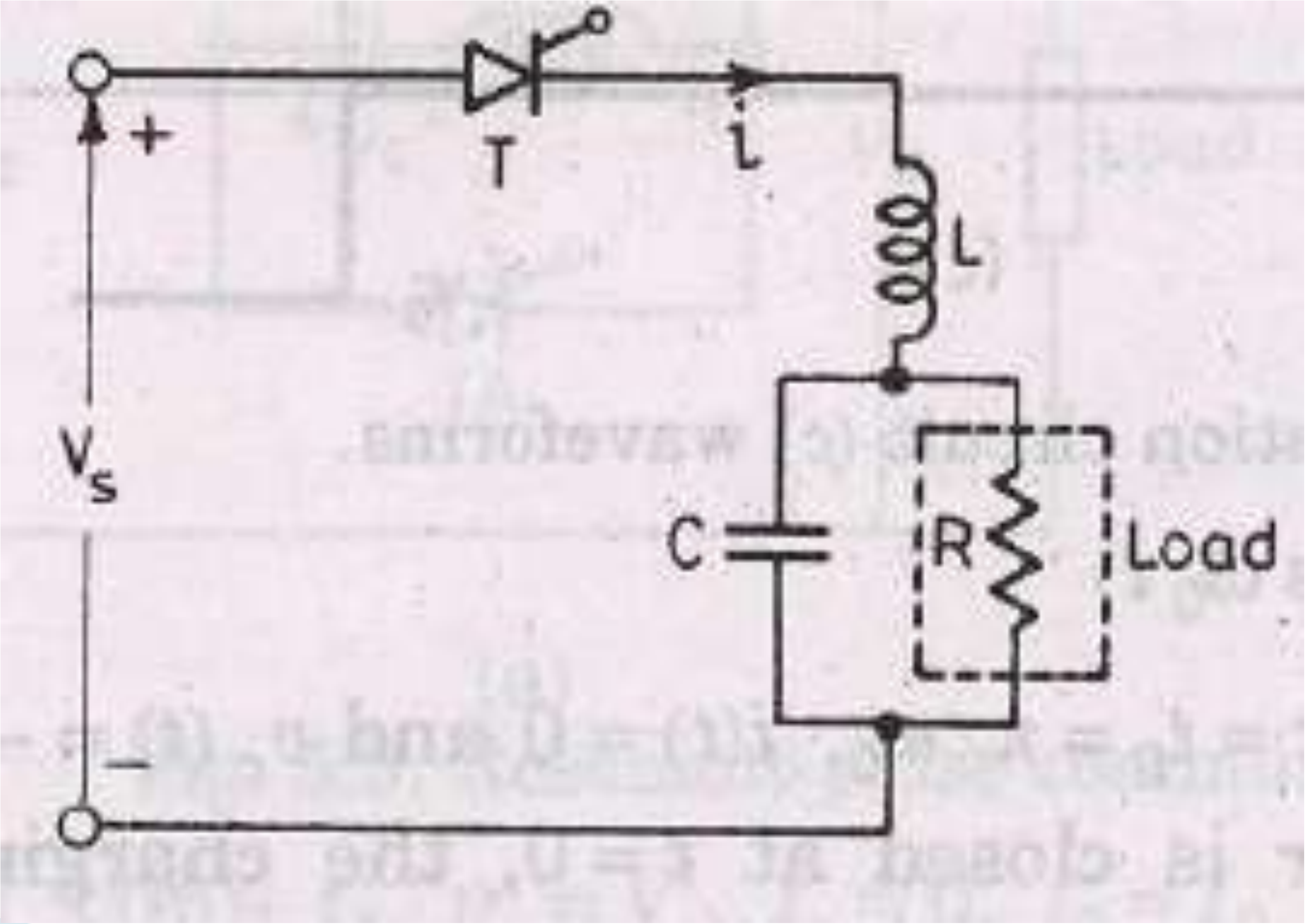
- UJT is highly efficient switch.
- Switching time is of the range of nano seconds.
- Because of negative resistance characteristics, UJT can be used as relaxation oscillator.
- External resistance R_1 and R_2 are small as compared to internal resistances R_{B1} and R_{B2}.
- On application of V_{BB}, capacitor C begins to charge through R, exponentially towards V_{BB}.

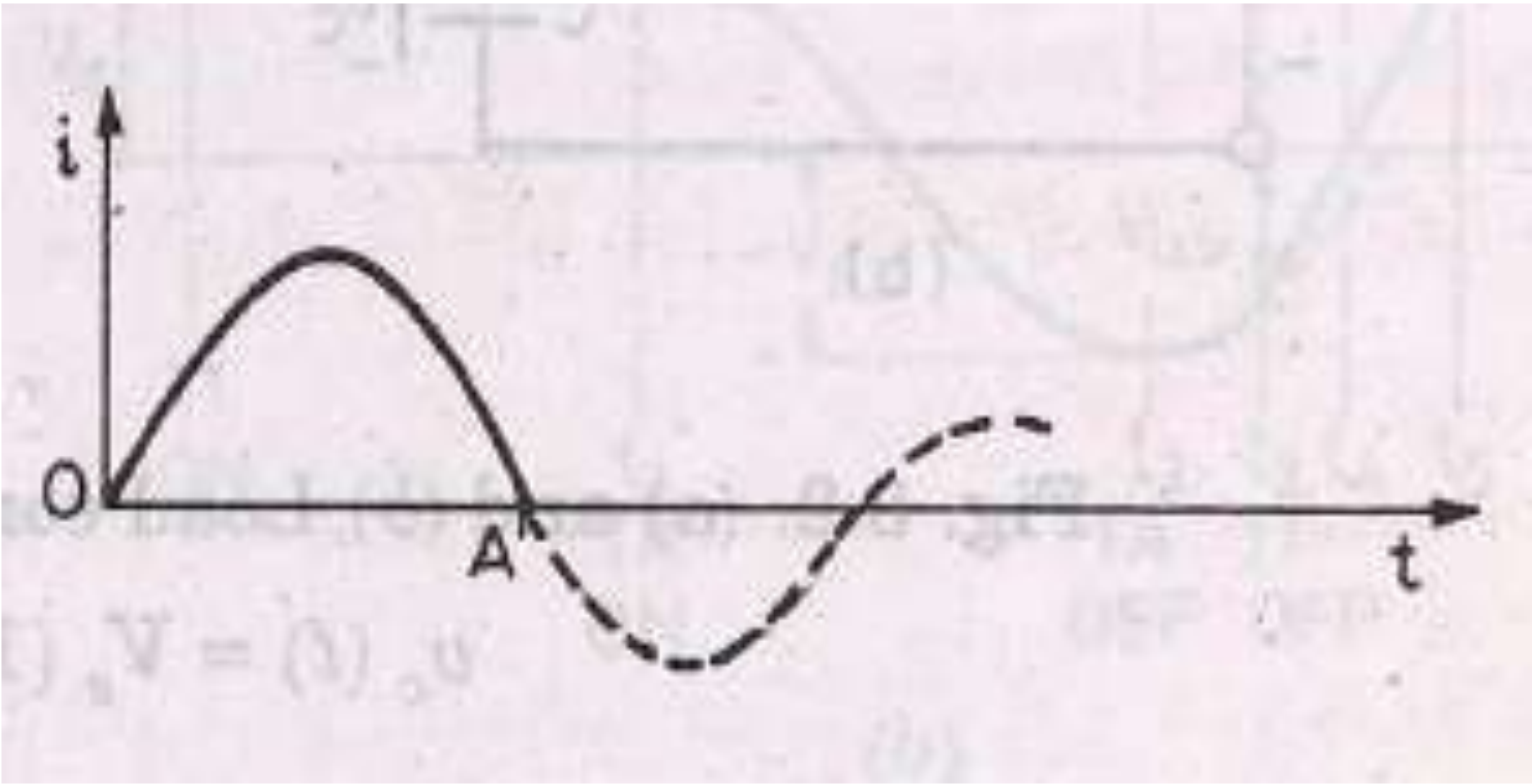
Commutation of Thyristor

Class A Commutation (Load Commutation)

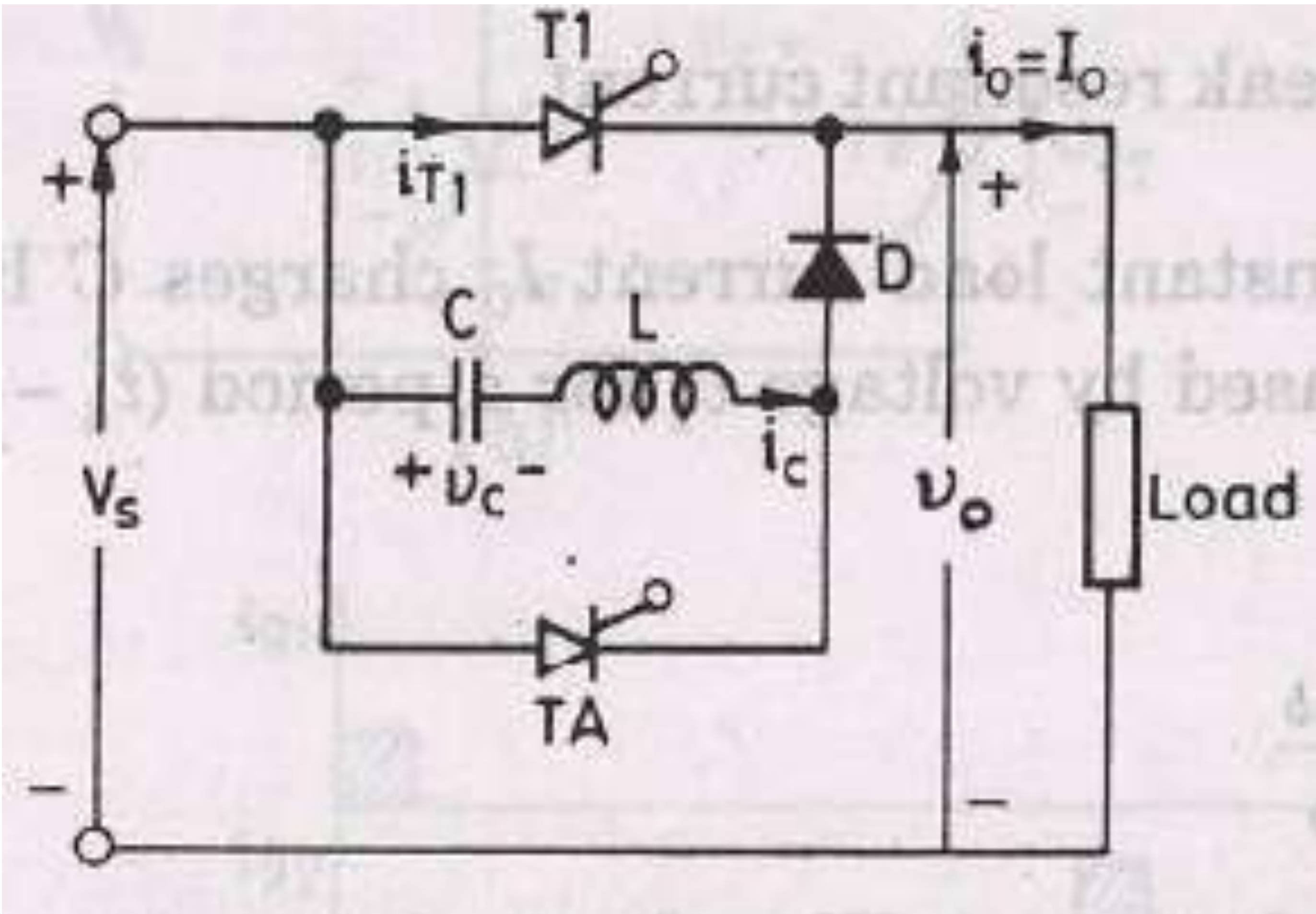



i
O
A
t

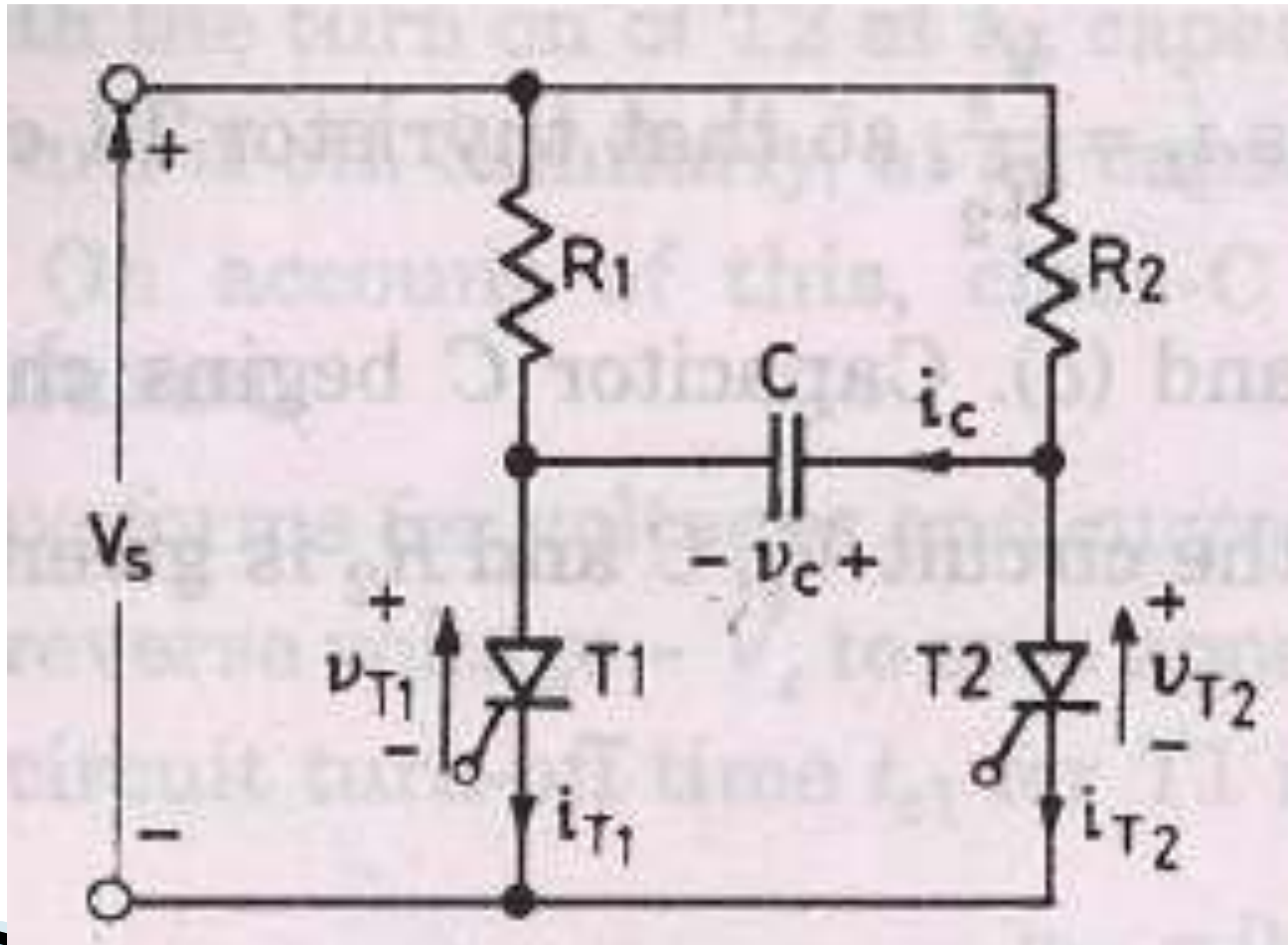

T
i
L
+
V
s
–
C
R
Load

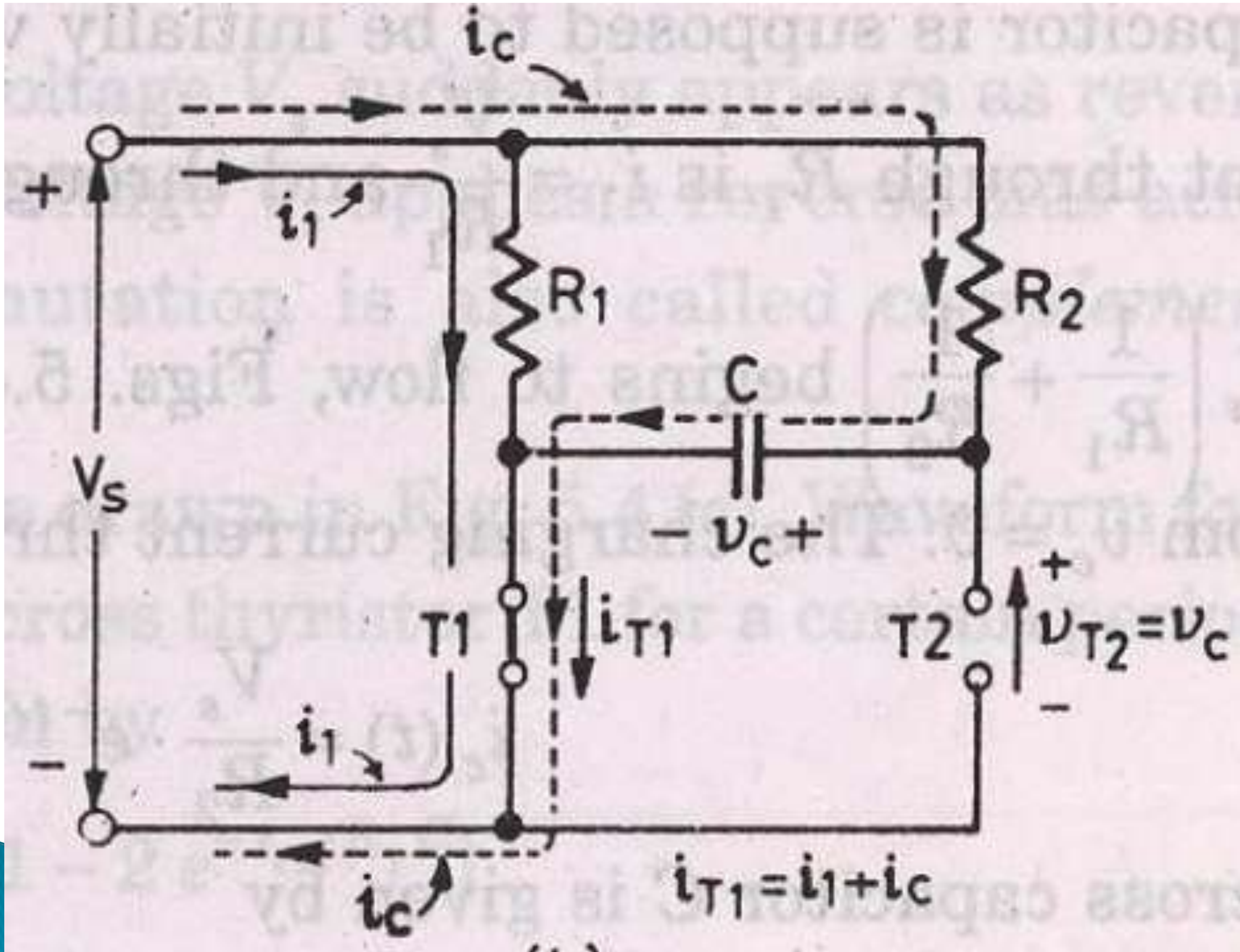

i
O
A
t

Class B Commutation (Resonant Pulse Commutation)



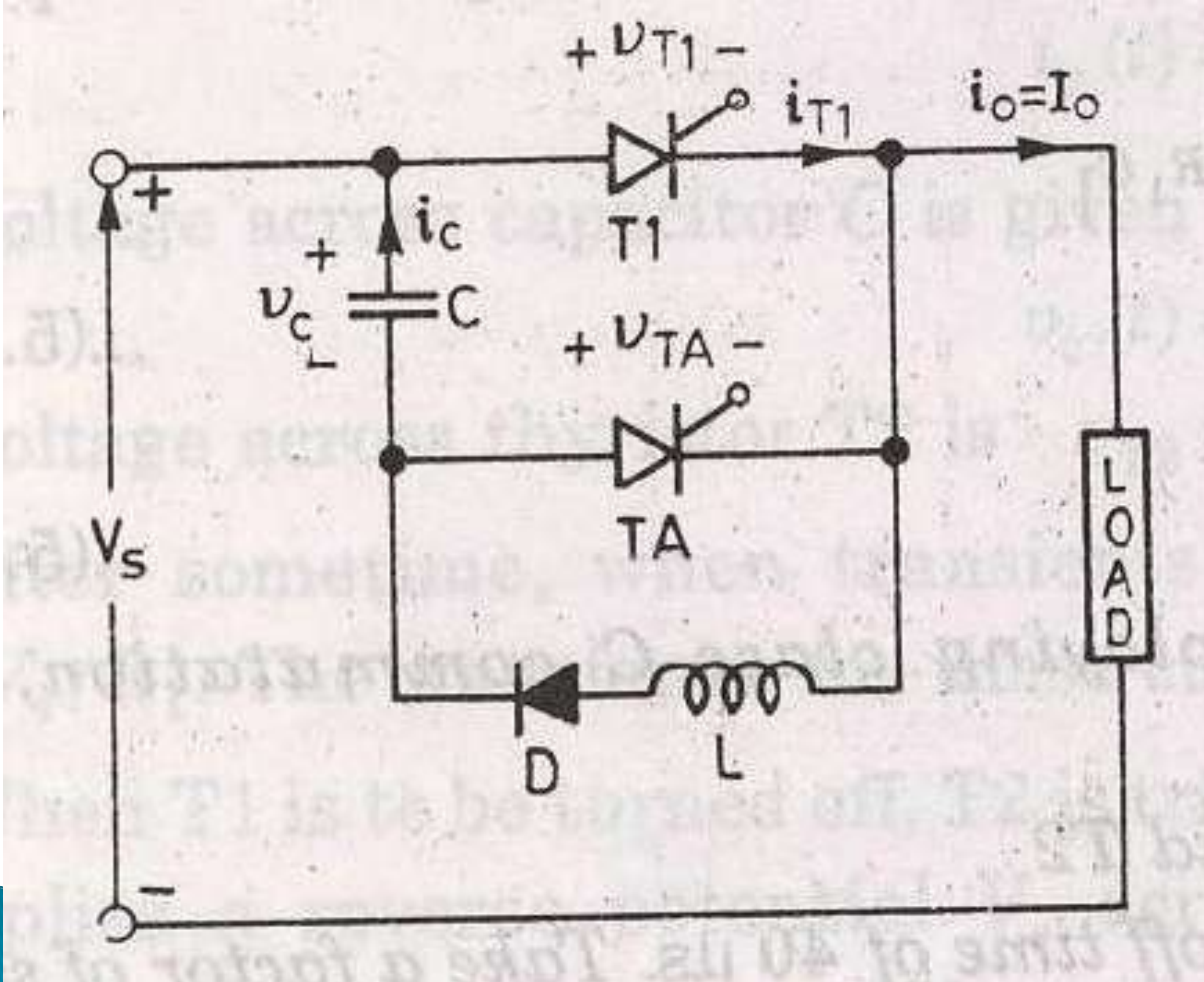
Class C Commutation (Complementry Commutation)





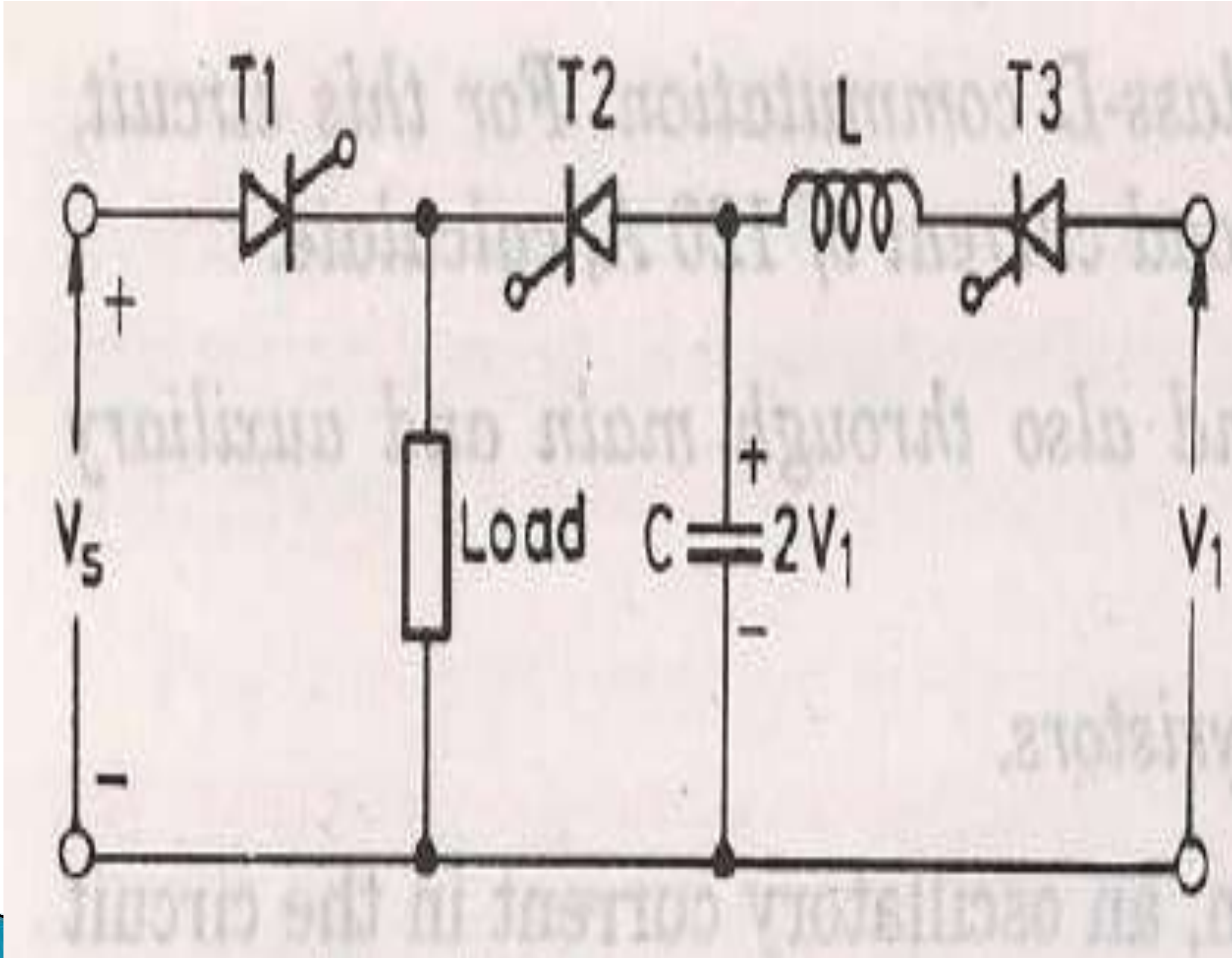
i_c
+
i_1
R_1
R_2
C
V_S
$- v_c +$
T1
i_{T1}
T2
+
$v_{T2} = v_c$
−
i_1
−
i_c
$i_{T1} = i_1 + i_c$

Class D Commutation: Impulse Commutation

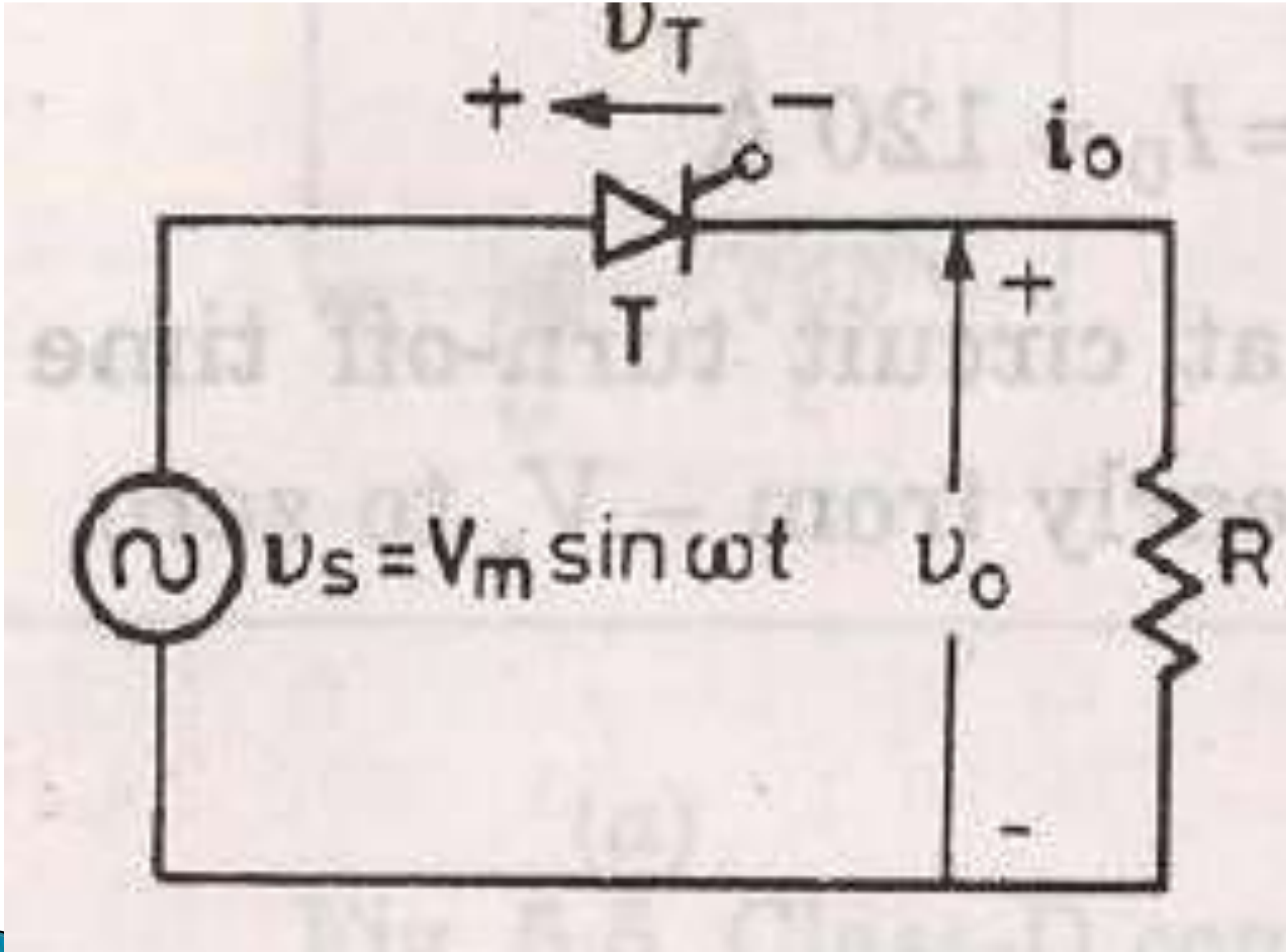


+ vT1 −
iT1
io=Io
+
ic
T1
+
vC
C
+ vTA −
TA
Vs
L
O
A
D
D
L
−

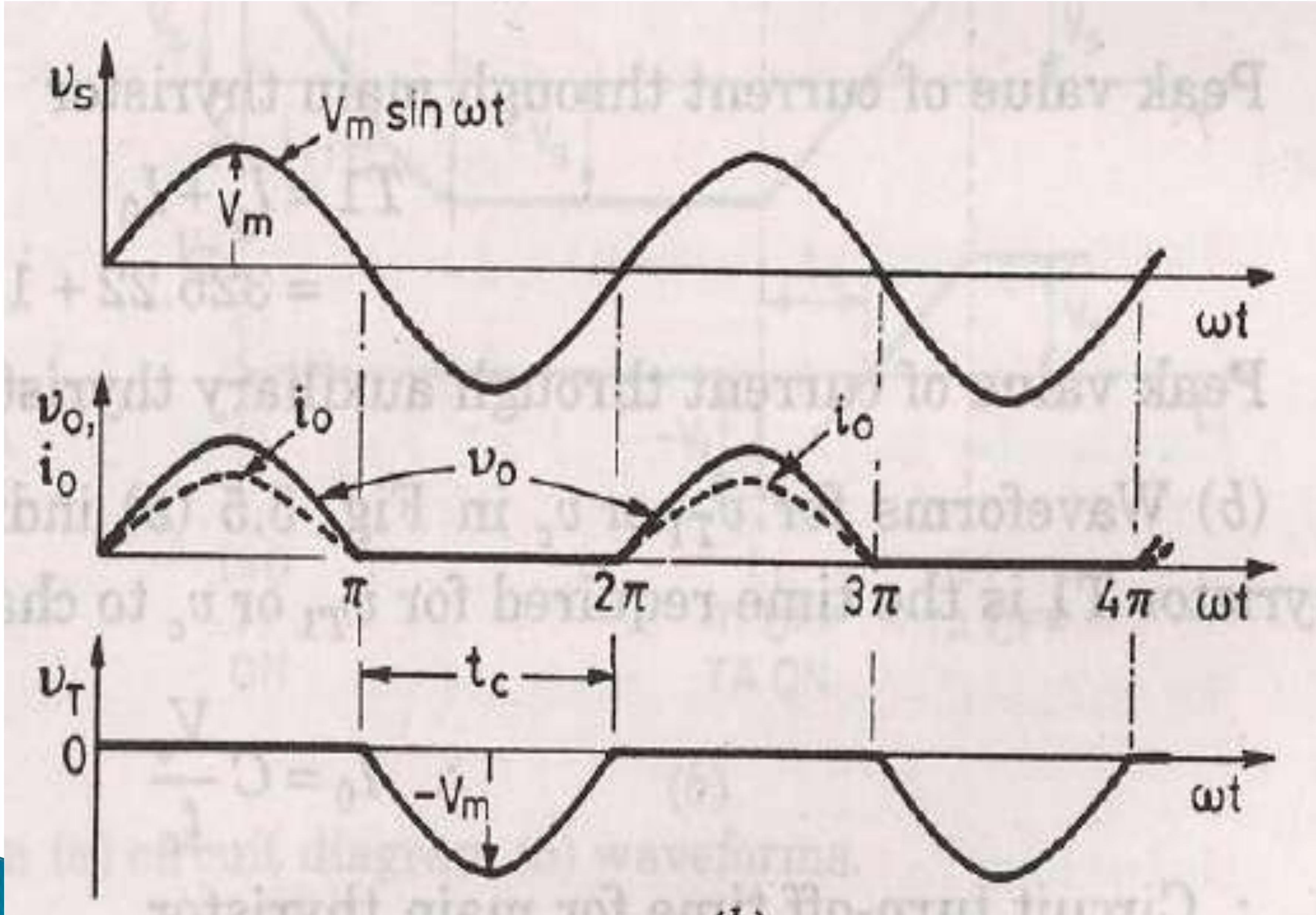
Class E Commutation: External Pulse Commutation


T1
T2
L
T3
+
Vs
−
Load
+
C
2V1
−
V1

Class F or Line Commutation



v_T
+
−
i_o
T
+
$v_s = V_m \sin \omega t$
v_o
R
-

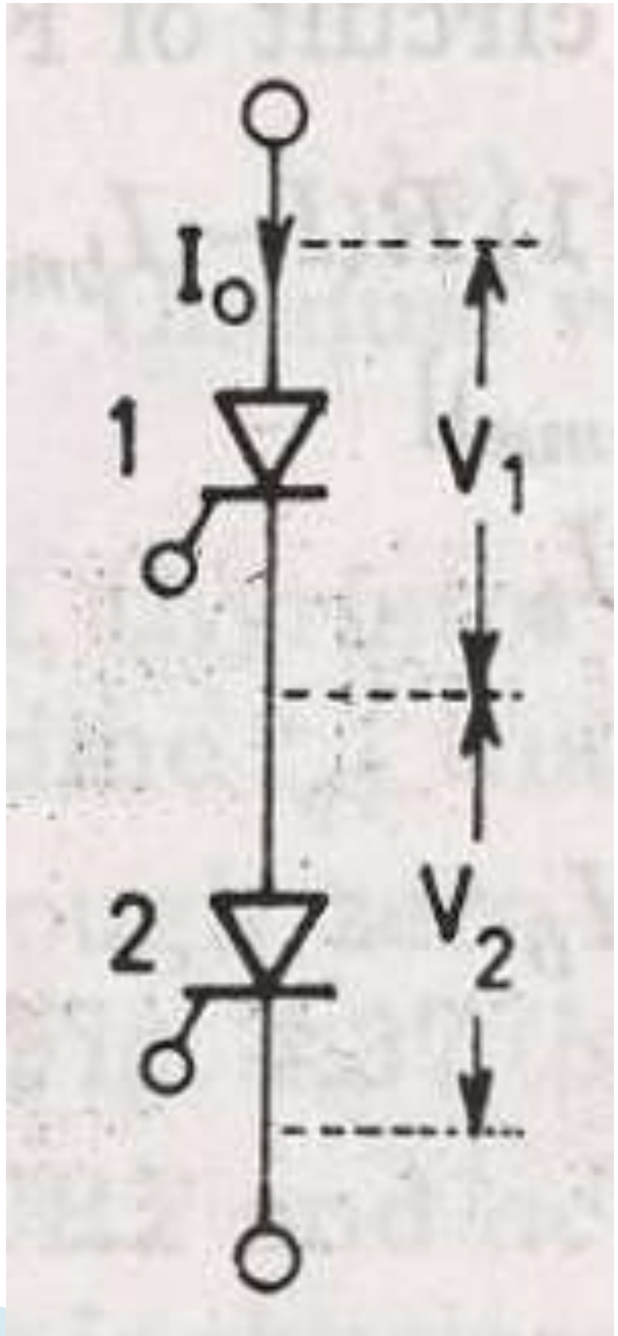

vS
Vm sin ωt
Vm
ωt
vO,
iO
iO
vO
iO
π
2π
3π
4π
ωt
vT
tc
0
-Vm
ωt

Series and Parallel Operation

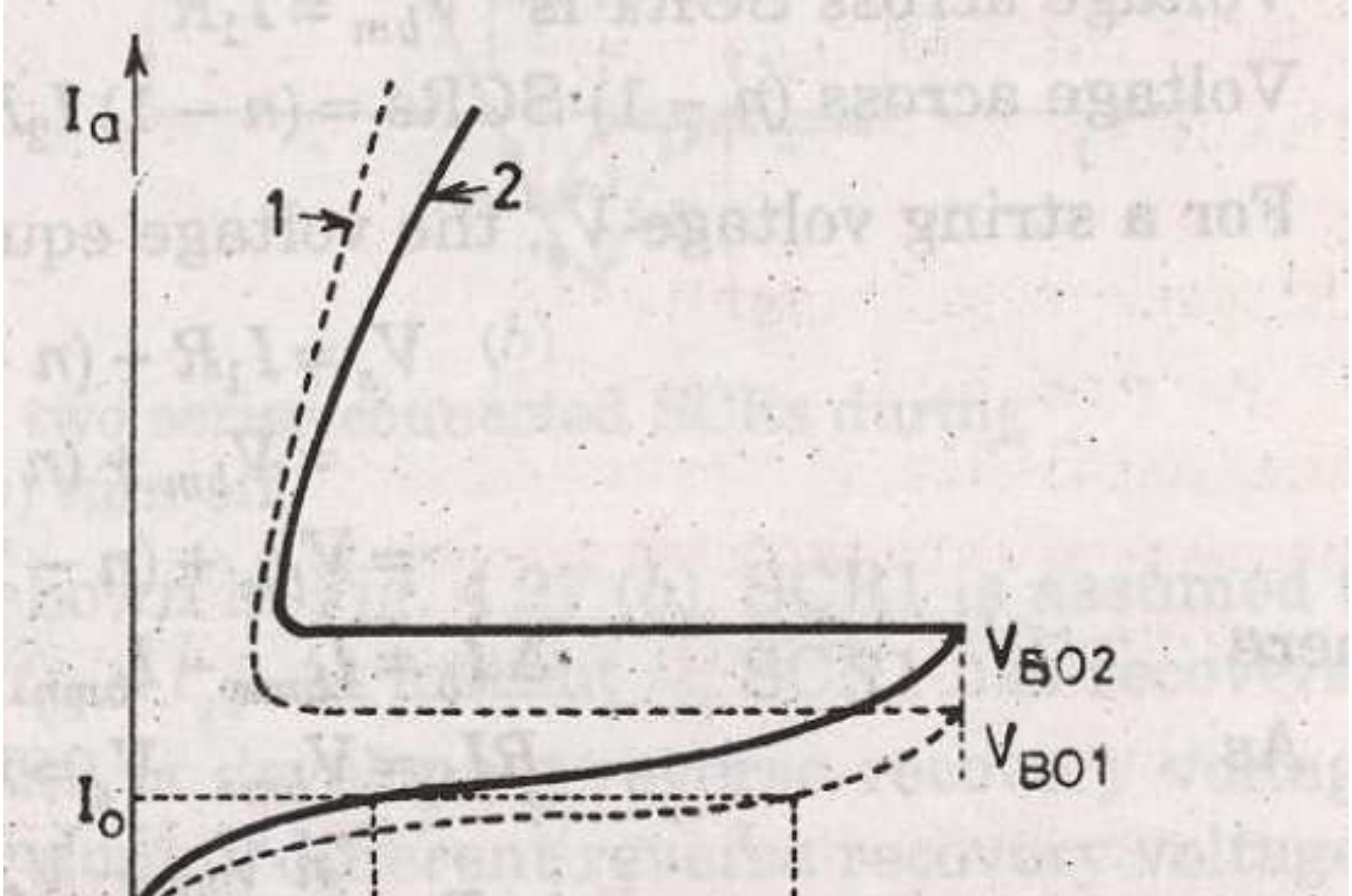
$$\text{string efficiency} = \frac{\text{Actual voltage/current rating of the whole string}}{[\text{Individual voltage/current rating of one SCR}]\,[\text{Number of SCRs in the string}]}$$

$$DRF = 1 - \text{string efficiency}$$

Series Operation

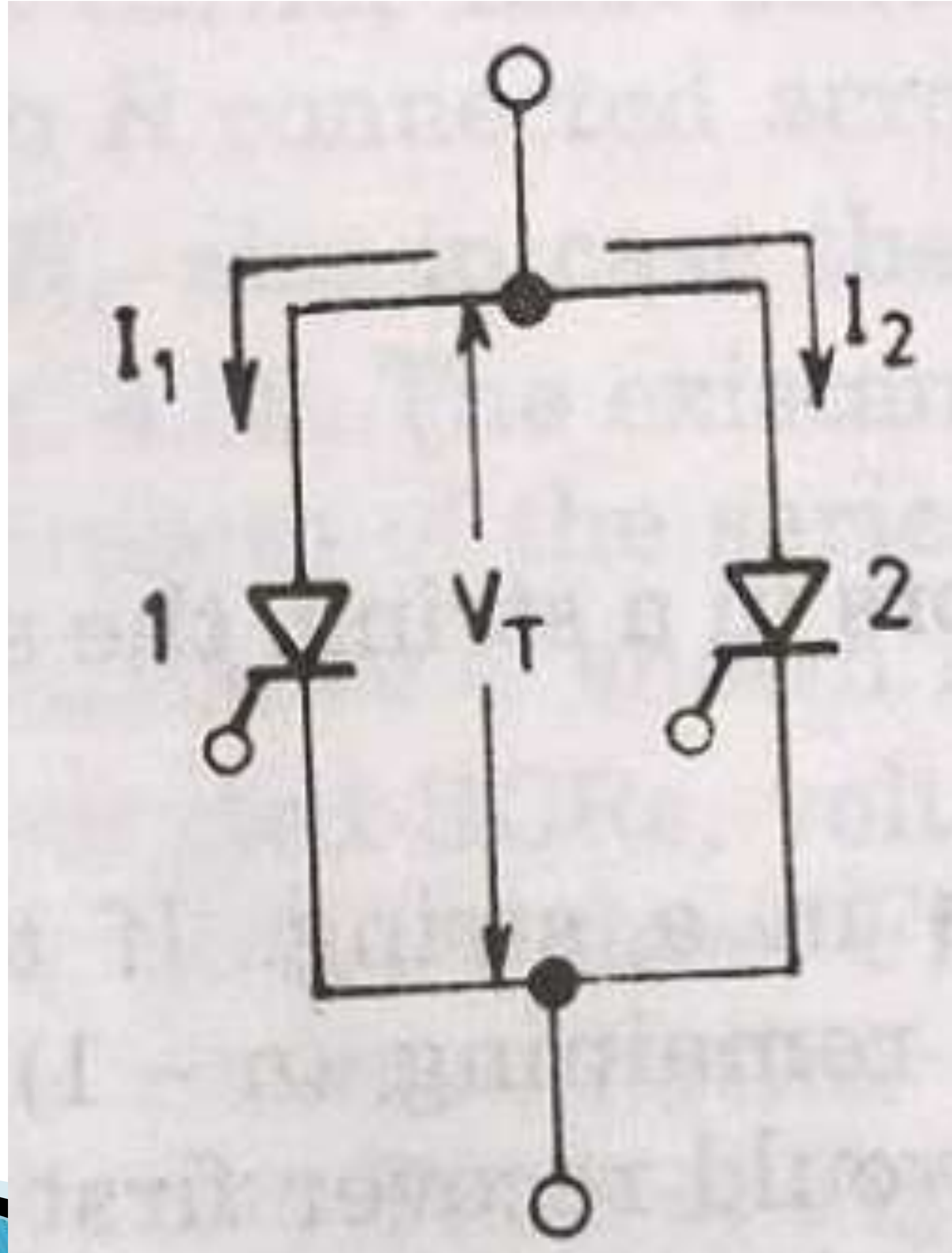


Io
1
2
V1
V2

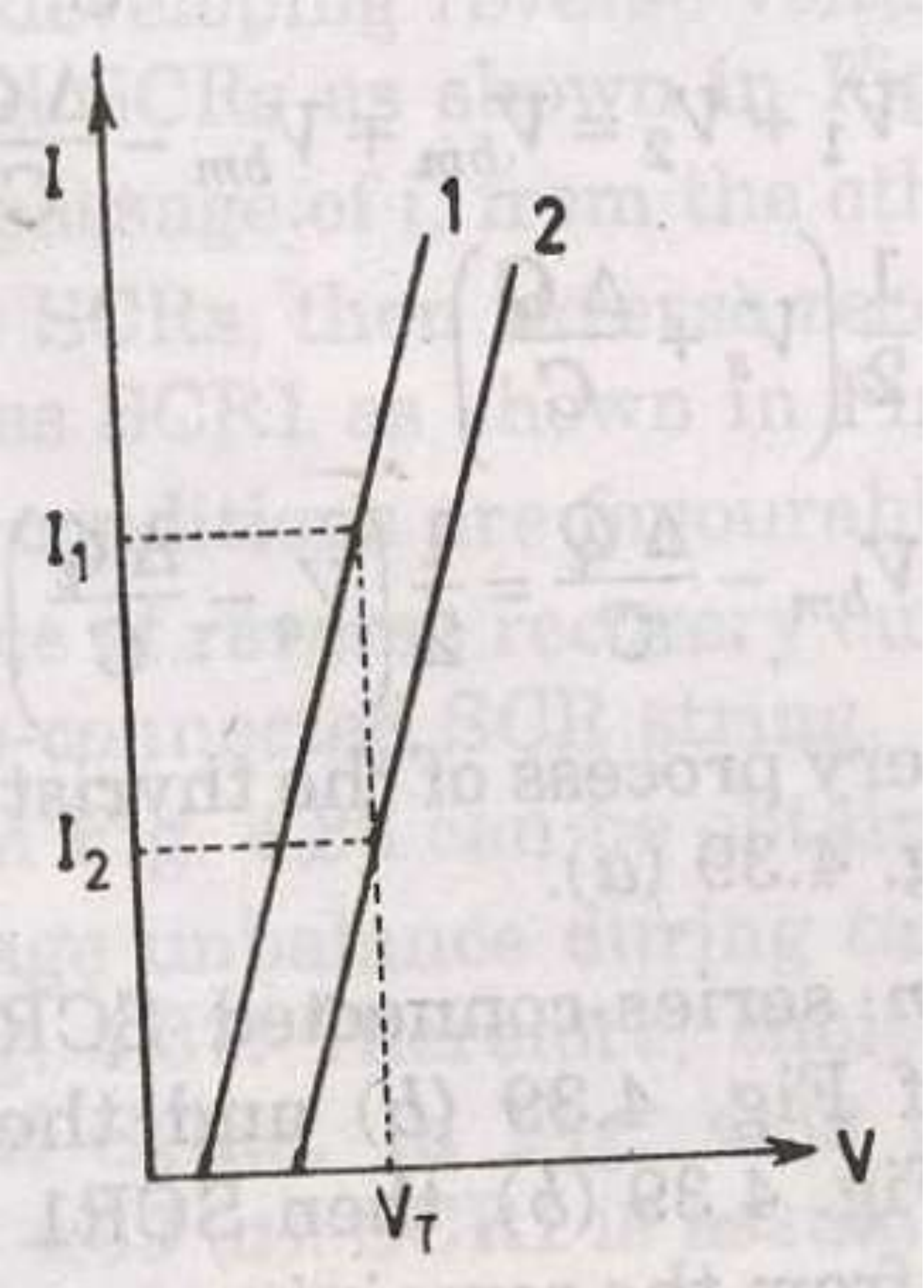


Ia
1
2
VBO2
VBO1
Io
V2
V1
Va

Parallel Operation



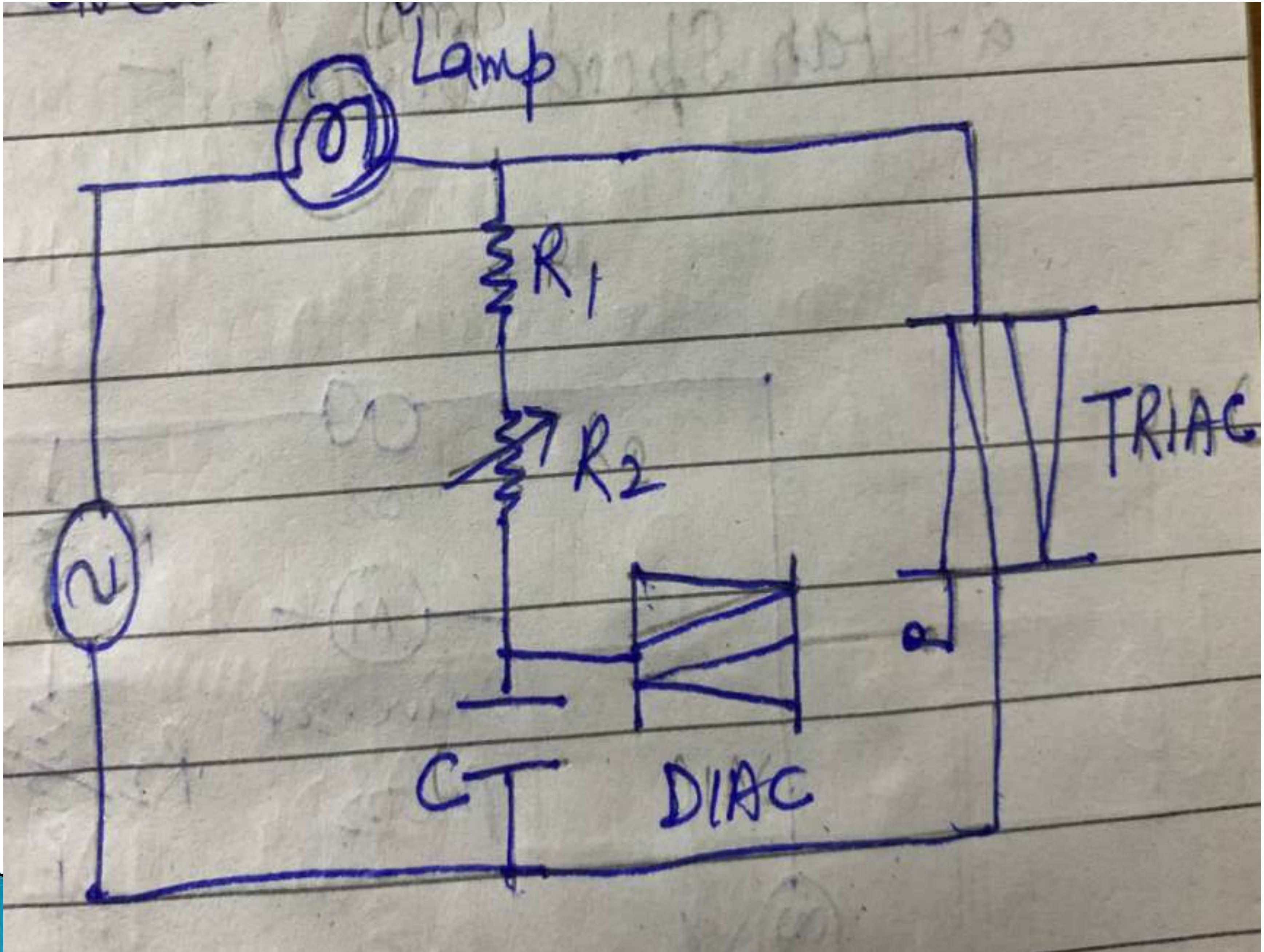
I1
I2
1
VT
2



I
1
2
I_1
I_2
V
V_T

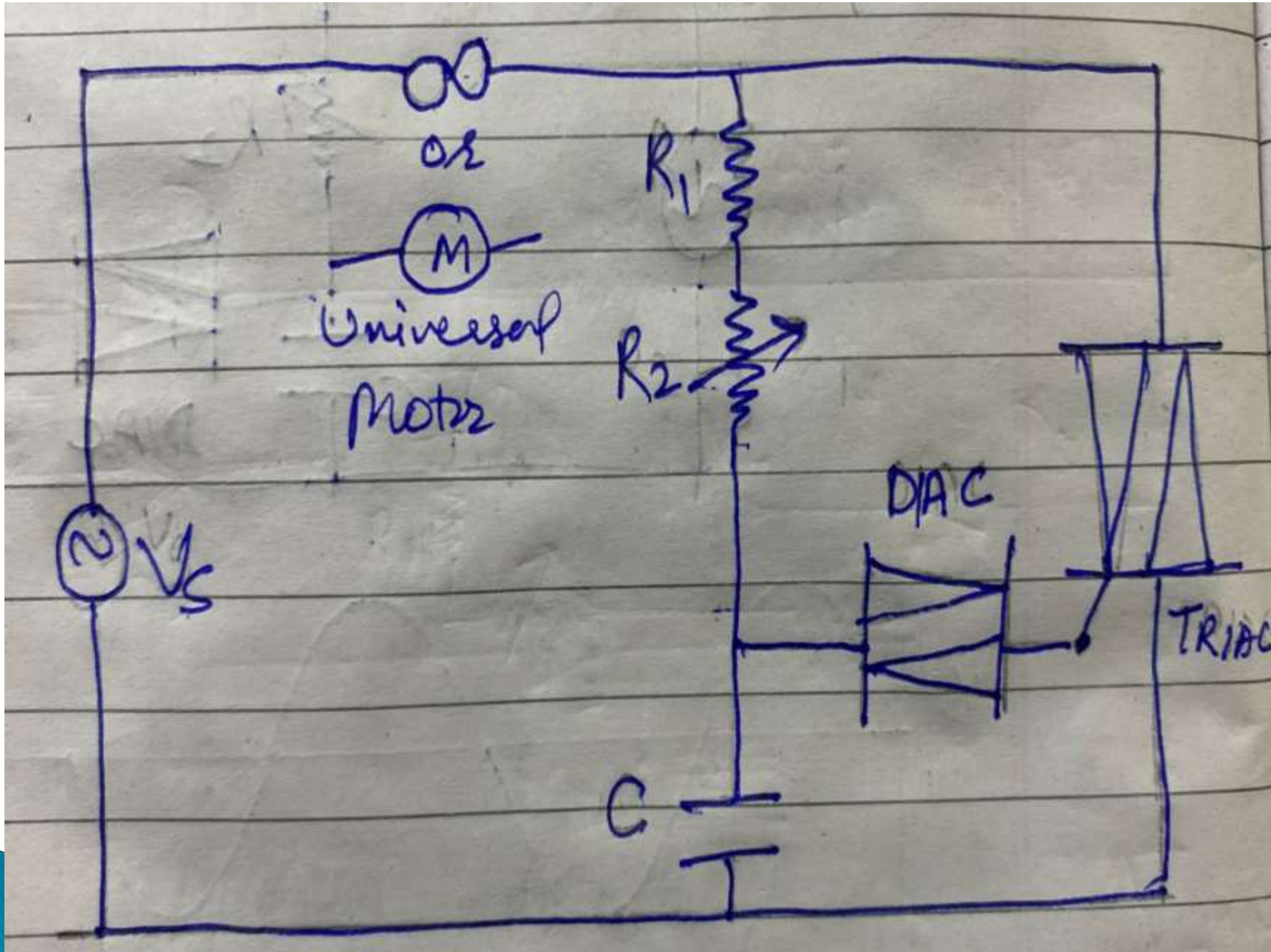
Applications of Thyristor

Light intensity Control



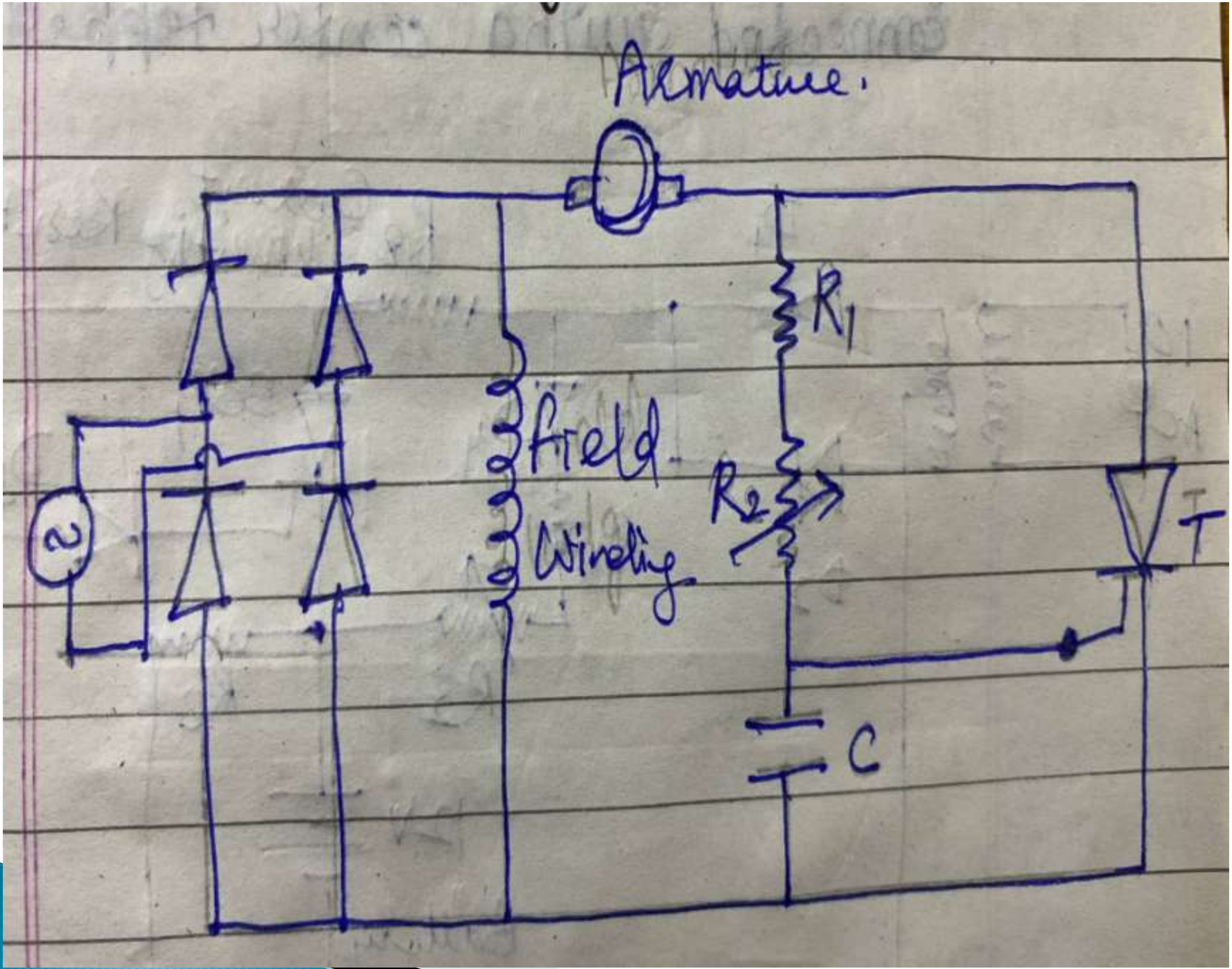
Lamp
R1
R2
TRIAC
C
DIAC

Fan Speed Cntrol

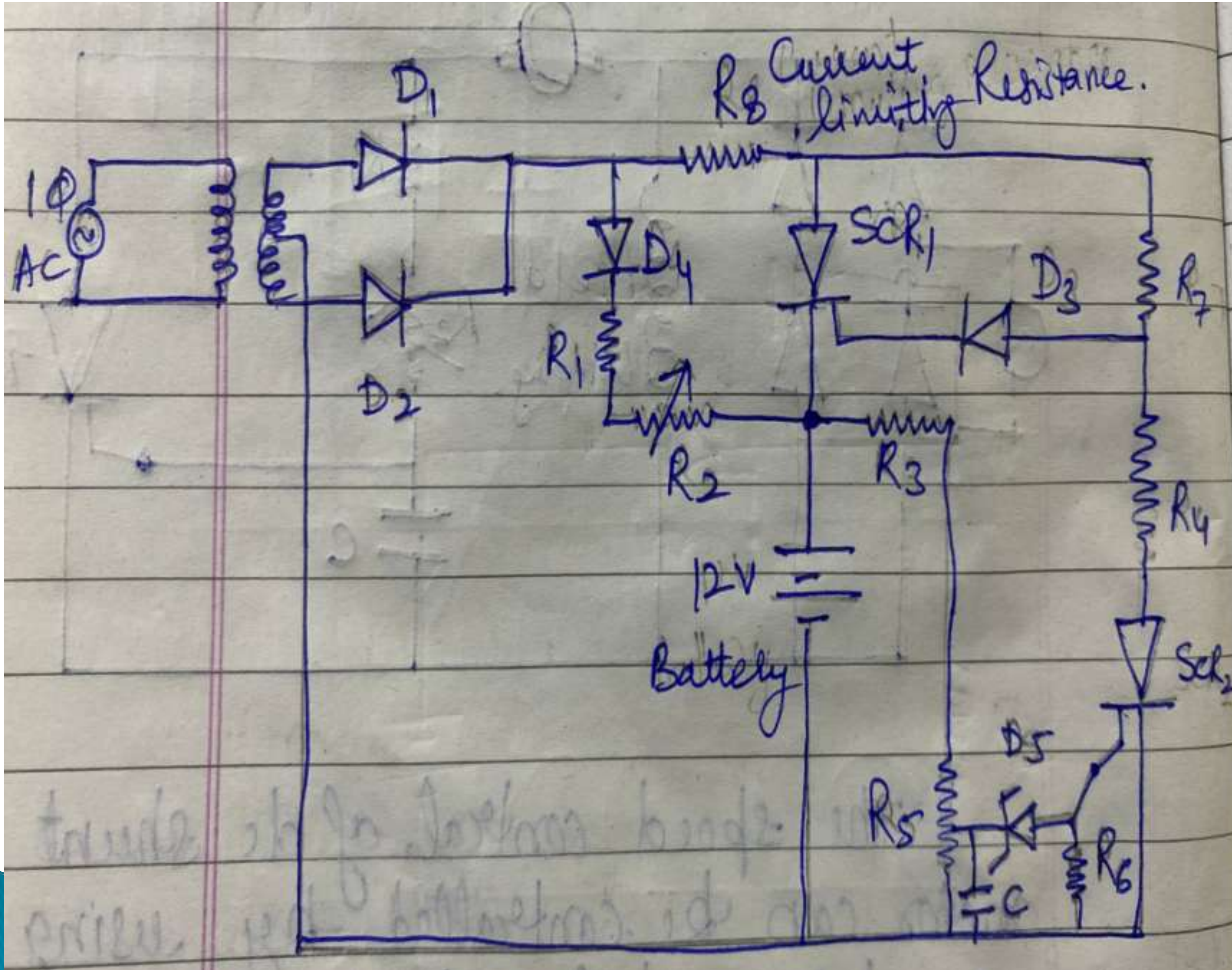


or
M
Universal
Motor
R1
R2
Vs
DIAC
TRIAC
C

Speed Control of DC Motor

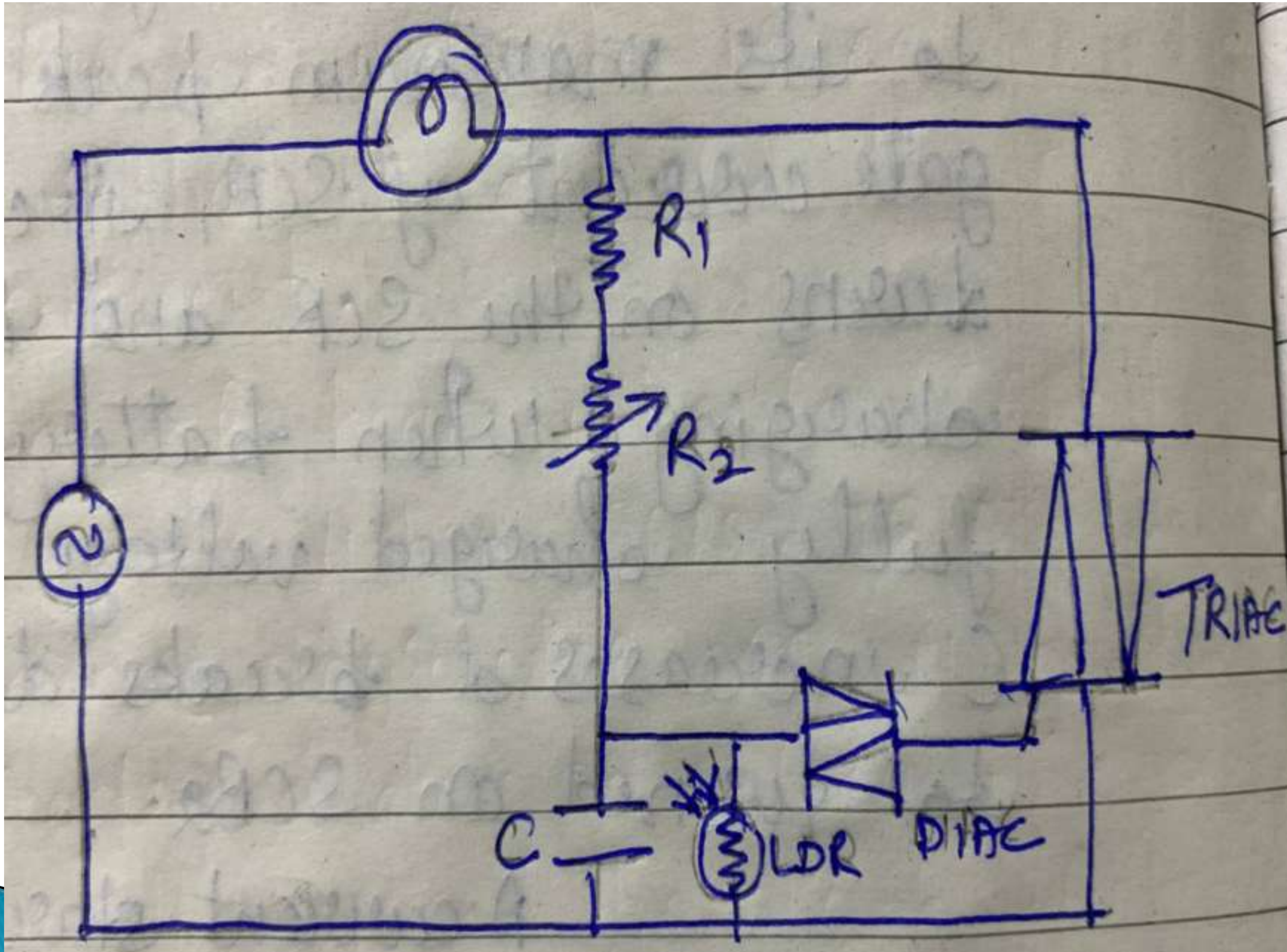

Armature.
R1
field
Winding
R2
T
C

Battery Charger



D1
R8
Current limiting Resistance.
1Φ
AC
D4
SCR1
D3
R7
R1
D2
R2
R3
R4
12V
Battery
Scr2
D5
R5
R6
C

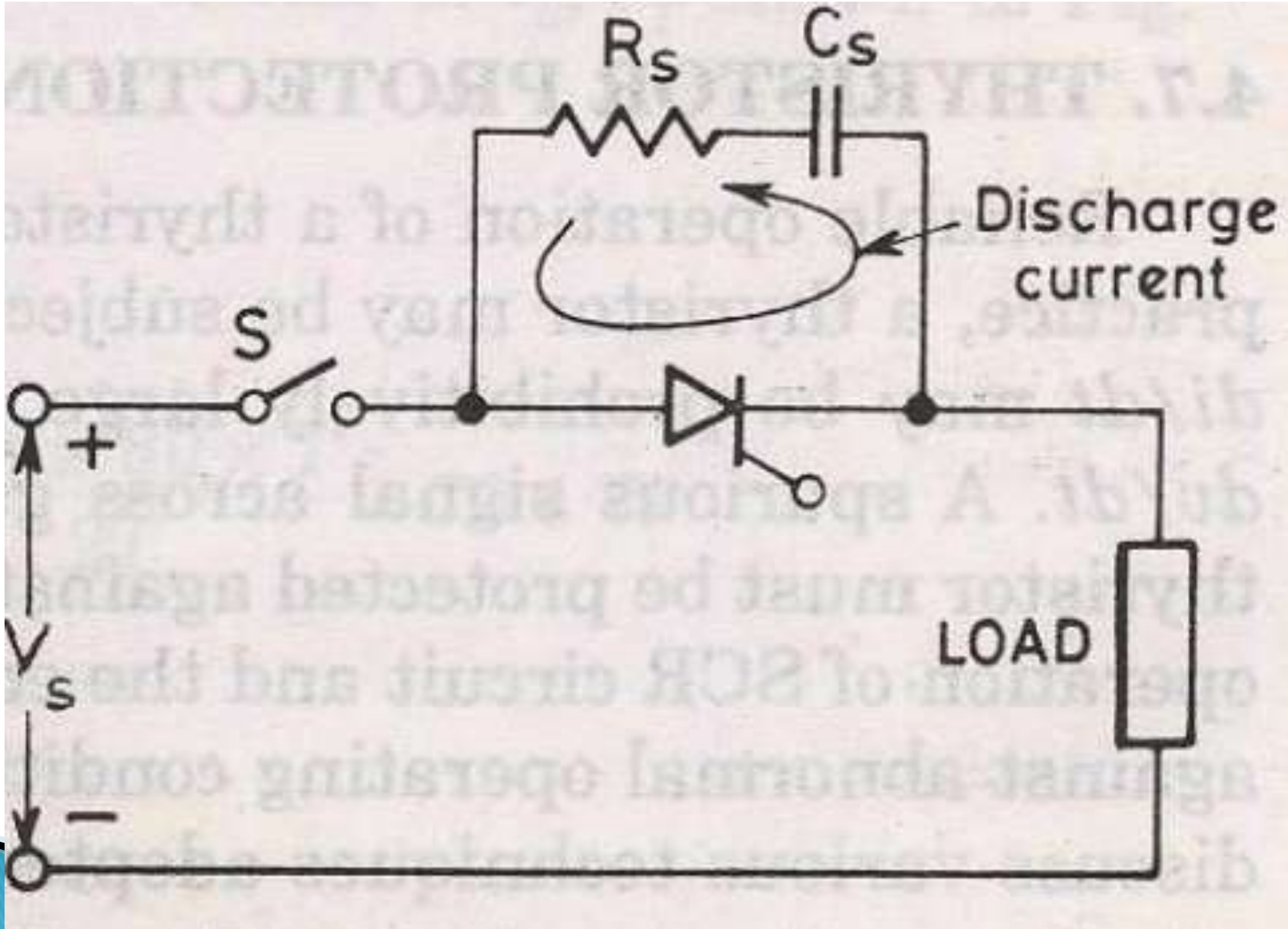
Automatic Street Light



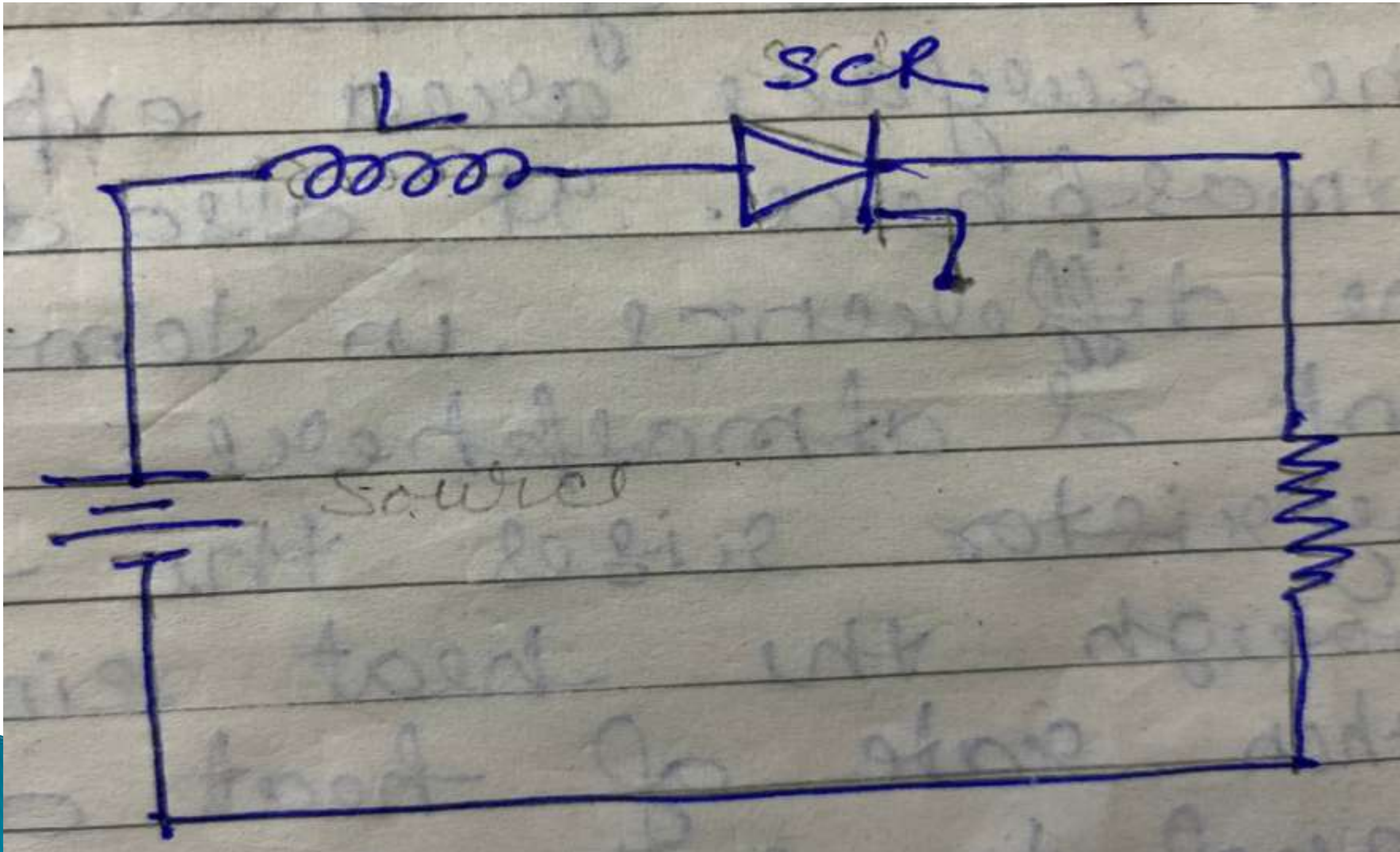
R1
R2
TRIAC
C
LDR
DIAC

SCR Protection

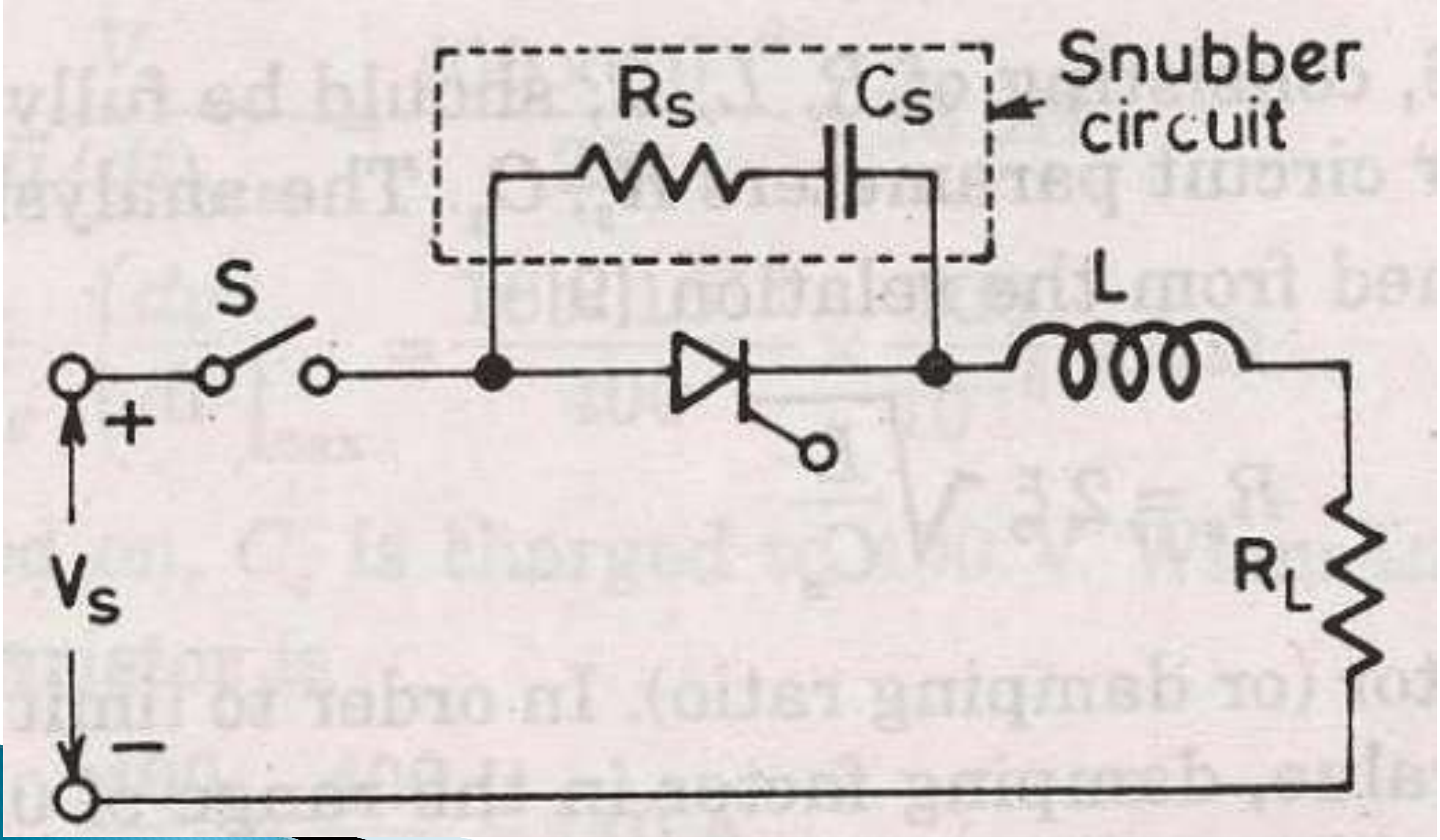
dv/dt Protection (Snubber Ckt)



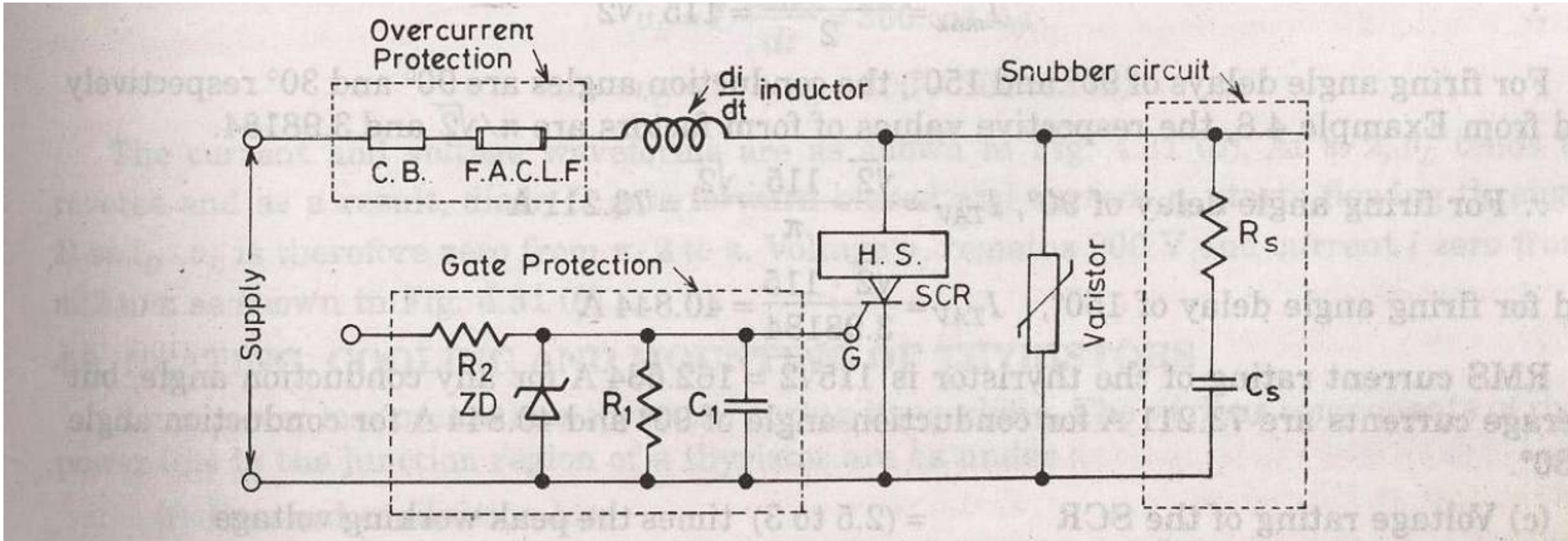
di/dt Protection



di/dt Protection



Complete Protection Ckt.



C.B.—Circuit breaker ; F.A.C.L.F.—Fast acting current limiting fuse ; H.S.—Heat sink ; ZD—Zener diode.